PHILIPS

Data handbook

Electronic components and materials

Components and materials

Part 5 July 1975

Ferrite core memory products

COMPONENTS AND MATERIALS

Part 5

July 1975

Ferroxcube memory cores	A
Matrix planes and stacks	B
Core memory systems	C
Maintenance type list and contents	

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CARACAS

DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, subassemblies and materials; it is made up of three series of handbooks each comprising several parts.

ELECTRON TUBES	**BLUE**
SEMICONDUCTORS AND INTEGRATED CIRCUITS	**RED**
COMPONENTS AND MATERIALS	**GREEN**

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

December 1972

ELECTRON TUBES (BLUE SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1a Transmitting tubes for communications and Tubes for r.f. heating Types PB2/500 ÷ TBW15/125 — **April 1973**

Part 1b Transmitting tubes for communication
Tubes for r.f. heating
Amplifier circuit assemblies — **August 1974**

Part 2 Microwave products — **October 1974**

Communication magnetrons
Magnetrons for micro-wave heating
Klystrons
Traveling-wave tubes
Diodes
Triodes
T-R Switches
Microwave Semiconductor devices
Isolators Circulators

Part 3 Special Quality tubes;
Miscellaneous devices — **January 1975**

Part 4 Receiving tubes — **March 1975**

Part 5a Cathode-ray tubes — **April 1975**

Part 5b Camera tubes; Image intensifier tubes — **May 1975**

Part 6 Products for nuclear technology
Photodiodes — **January 1974**

Photomultiplier tubes
Channel electron multipliers
Geiger-Mueller tubes
Neutron tubes
Photodiodes

Part 7 Gas-filled tubes — **February 1974**

Voltage stabilizing and reference tubes
Counter, selector, and indicator tubes
Trigger tubes
Switching diodes
Thyratrons
Ignitrons
Industrial rectifying tubes
High-voltage rectifying tubes

Part 8 T.V. Picture tubes — **May 1974**

SEMICONDUCTORS AND INTEGRATED CIRCUITS (RED SERIES)

This series consists of the following parts, issued on the dates indicated.

Part 1a Rectifier diodes and thyristors — **June 1974**

Rectifier diodes
Voltage regulator diodes (> 1,5 W)
Transient suppressor diodes
Thyristors, diacs, triacs
Rectifier stacks

Part 1b Diodes — **July 1974**

Small signal germanium diodes
Small signal silicon diodes
Special diodes
Voltage regulator diodes (< 1,5 W)
Voltage reference diodes
Tuner diodes

Part 2 Low frequency transistors — **July 1974**

Part 3 High frequency and switching transistors — **October 1974**

Part 4a Special semiconductors — **November 1974**

Transmitting transistors
Microwave devices
Field-effect transistors
Dual transistors
Microminiature devices for thick- and thin-film circuits

Part 4b Devices for opto-electronics — **December 1974**

Photosensitive diodes and transistors
Light emitting diodes
Photocouplers
Infra-red sensitive devices
Photoconductive devices

Part 5 Linear integrated circuits — **March 1975**

Part 6 Digital integrated circuits — **April 1974**

DTL (FC family)
CML (GX family)
MOS (FD family)
MOS (FE family)

COMPONENTS AND MATERIALS (GREEN SERIES)

These series consists of the following parts, issued on the dates indicated.

Part 1 Functional units, Input/output devices, Electro-mechanical components, Peripheral devices **June 1974**

High noise immunity logic FZ/30-Series
Circuit blocks 40-Series and CSA70
Counter modules 50-Series
Norbits 60-Series, 61-Series
Circuit blocks 90-Series
Input/output devices
Electro-mechanical components
Peripheral devices

Part 2a Resistors **September 1974**

Fixed resistors
Variable resistors
Voltage dependent resistors (VDR)
Light dependent resistors (LDR)
Negative temperature coefficient thermistors (NTC)
Positive temperature coefficient thermistors (PTC)
Test switches

Part 2b Capacitors **November 1974**

Electrolytic and solid capacitors
Paper capacitors and film capacitors
Ceramic capacitors
Variable capacitors

Part 3 Radio, Audio, Television **February 1975**

FM tuners
Loudspeakers
Television tuners, aerial input assemblies
Components for black and white television
Components for colour television *)

Part 4a Soft ferrites **April 1975**

Ferrites for radio, audio and television
Beads and chokes
Ferroxcube potcores and square cores
Ferroxcube transformer cores

Part 4b Piezoelectric ceramics, Permanent magnet materials **May 1975**

Part 5 Ferrite core memory products **July 1975**

Ferroxcube memory cores
Matrix planes and stacks
Core memory systems **)

Part 6 Electric motors and accessories **March 1974**

Small synchronous motors
Stepper motors
Miniature direct current motors

Part 7 Circuit blocks **September 1971**

Circuit blocks 100 kHz-Series
Circuit blocks 1-Series
Circuit blocks 10-Series
Circuit blocks for ferrite core memory drive

Part 8 Variable mains transformers **July 1975**

*) Deflection assemblies for camera tubes are now included in handbook series "Electron tubes", Part 5b.

**) For detailed information on "Piezoelectric quartz devices" consult the Product Data booklet No. 9399 432 01301.

Ferroxcube memory cores

STANDARD RANGE

core type	old type number	temperature range	C4 [1]	nominal operating conditions T_{amb} = 25 °C, D.R. = 0,50			relevant typical output characteristics V_{ref} = 0,1 rV_1				
				I	t_r	t_d	uV_1	rV_1	wV_z	t_p	t_s
			(mA/°C)	(mA)	(μs)	(μs)	(mV)	(mV)	(mV)	(μs)	(μs)
18H51	–	medium	1,3	555	0,05	0,30	45	44	5	0,120	0,240
18H53 [2]	–	medium	1,3	560	0,05	0,30	45	44	4,5	0,135	0,250
18H61	–	medium	1,4	644	0,05	0,25	55	53	5	0,110	0,210
18H81	6H11	medium	2,0	800	0,05	0,20	66	64	6	0,095	0,170
18H83	–	medium	2,0	833	0,05	0,30	55	54	4	0,105	0,190
18H86	6H6	standard	1,3	825	0,05	0,21	53	52	5	0,095	0,175
20H74	6H4	standard	2,7	710	0,05	0,26	66	63	5	0,110	0,220
20H83 [3]	6H3	standard	3,5	890	0,05	0,23	49	48	4	0,105	0,190
20H85 [3]	6H5	medium	1,6	865	0,05	0,23	65	63	8	0,100	0,190
20H89	6H9	medium	2,0	800	0,05	0,25	64	61	8,5	0,110	0,210
20H92	6H2	medium	1,4	973	0,05	0,26	52	51	4	0,110	0,210
30F78	6F8	standard	3,1	710	0,1	0,50	63	61	5	0,200	0,40
30F83	6F3	medium	1,3	800	0,15	0,59	68	67	5	0,270	0,49
50C51 [3]	6C1	standard	2,3	530	0,2	1,1	63	60	8	0,46	0,87
50C82 [3]	6C2	medium	1,1	805	0,25	1,2	100	98	7	0,45	1,00
50D35 [3]	6D5	standard	2,4	395	0,2	1,5	64	62	9	0,58	1,18
50D49 [3]	6D9	standard	1,5	475	0,2	1,5	60	58	8	0,55	1,20
150E31 [3]	6E1	standard	2,7	385	0,8	12	115	110	22	2,9	6,4

150E31 — (internal ref. no.)
- 1 — first figure of nominal current at 25 °C
- E — basic ferroxcube grade
- 150 — outer dia in mil

Notes:

1) Rate of change of full drive current for constant uV_1.

2) Data sheet available separately.

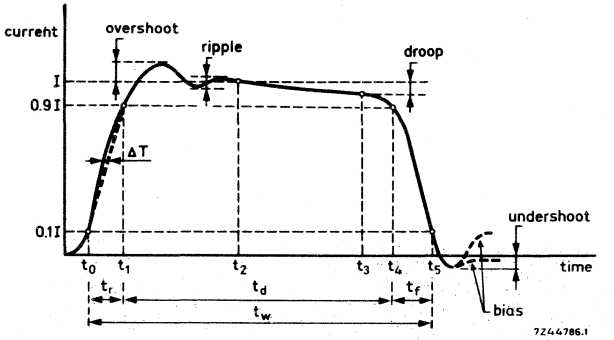
3) Maintenance type.

INTRODUCTION

CORE CHARACTERISTICS

The characteristic properties of a Ferroxcube Memory Core are described in terms of its response to a set of defined test conditions. Under these test conditions, the core is effectively coupled to two circuits, drive current pulses being carried by one and response voltage pulses being induced in the other. The two circuits are so arranged that, in the absence of a core, negligible coupling exists between them.

THE CURRENT PULSE, used in the measurement of memory cores.



The following definitions apply to the current pulse which is used in the measurement of Memory Cores.

Amplitude

I The magnitude of the current pulse immediately after the leading edge transients (overshoot and ripple) have decreased to less than 0.1% of the current magnitude.

Times

t_0 Time origin. The time when the leading edge of the current pulse reaches 10% of the amplitude of the current pulse.

t_1 The time when the leading edge of the current pulse first reaches 90% of the amplitude of the current pulse.

t_2 The time when the leading edge transients have decreased to less than 0.1% of the current magnitude.

t_3 The time for the end of the straight part of the top of the pulse.

t_4 The time when the trailing edge of the current pulse reaches 90% of the amplitude of the current pulse.

t_5 The time when the trailing edge of the current pulse reaches 10% of the amplitude of the current pulse.

Time intervals

t_r Rise time, the time interval $t_0 - t_1$

t_d Pulse duration, the time interval $t_1 - t_4$

t_f Decay time (Fall time), the time interval $t_4 - t_5$

Linearity of leading edge

Over the region t_0 to t_1, the maximum deviation in time of the actual pulse from a straight line joining the 10% and 90% points, expressed as a percentage of the rise time. For measurement purposes this is less than 2%.

Overshoot

The extent to which the maximum instantaneous current exceeds the Pulse Amplitude I, expressed as a percentage of I. For measurement purposes this is less than 1%.

Ripple

When the overshoot is followed by a damped oscillation this is known as ripple, this effect should be less than 1% for measurement purposes.

Droop

The decrease in current over the time interval t_2 to t_3 expressed as a percentage of I, per microsecond. For measurement purposes this is less than 1% per μs.

Undershoot

The maximum instantaneous value of the reverse current swing following the trailing edge of the pulse, expressed as a percentage of I. For measurement purposes, this is normally less than 1%.

Bias

A residual current flowing at all times in the test circuit. For measurement purposes this is less than 1%.

The Exponential pulse

When used, this pulse is defined in terms of the constants of the generating circuit.

Kinds of current pulses

I_r Full Read Pulse

The current pulse which, when applied to a core in the "one" state, will leave it in the "zero" state.

I_w Full Write Pulse

The current pulse which, when applied to a core in the "zero" state, will leave it in the "one" state. This corresponds to the superimposed partial write selection pulses in a coincident current matrix.

I_{pr} Partial Read Pulse

A pulse of the same polarity as the Full Read Pulse which, when applied to a core in the "one" state, is insufficient in amplitude to bring it to the "zero" state.

I_{pw} Partial Write Pulse

A pulse of the same polarity as the Full Write Pulse which, when applied to a core in the "zero" state, is insufficient in amplitude to bring it to the "one" state.

$D.R.$ Disturb Ratio

The ratio of the amplitude of the Partial Read or Write Pulse to the amplitude of the full Read or Write Pulse. In a matrix working under ideal conditions, $I_{pw} = 0.5\ I_w$ and the Disturb Ratio = 0.5. For core measurement purposes, it is usual to consider the case where the Full Pulses are less than the recommended nominal and the Partial Pulses are greater than half the recommended Full Pulse.

For example: If the recommended full drive current is I_{nom} and if

$I_r = I_w = I_{nom} - 10\%$ and $I_{pr} = I_{pw} = 0.5\, I_{nom} + 10\%$

then $$D.R. = \frac{1.1\ (0.5\ I_{nom})}{0.9\ (I_{nom})} = \frac{0.55}{0.9} = 0.61$$

Notes The read and write pulses are of opposite polarity.
I_{nom} is used for the nominal value of a full current pulse.

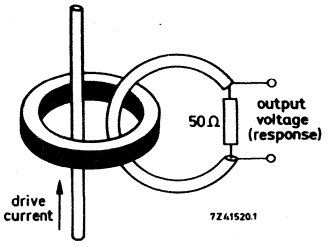
TEST CONDITIONS

All individual cores are tested upon meeting the specification on the relevant data sheet. Moreover, sample tests at several temperatures are carried out according to Mil Standard 105 D (inspection level II). An A.Q.L. of 0.015 is handled in testing cores of 30 mil and smaller.

Drive Pulses

Linear pulses are normally used and the amplitude and rise time of drive pulses are stated on the individual data sheets.

Deviation from linearity	< 2 %
Overshoot	< 1 %
Ripple	< 1 %
Droop	< 1 %
Undershoot	< 1 %
Bias	< 1 %



Sense Circuit

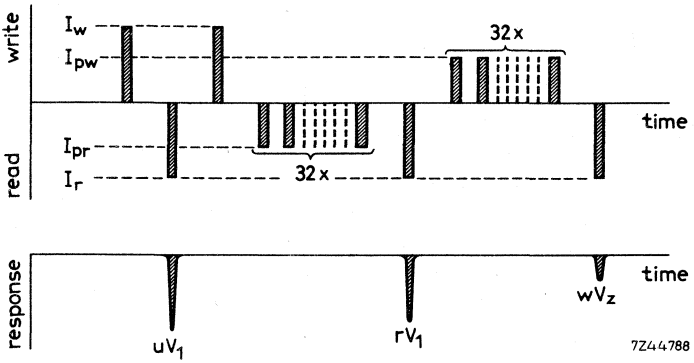
The core being measured is coupled to one turn of the sense circuit, this being terminated in 50 Ω.

Temperature

The temperatures at which core properties have been measured is stated on the individual data sheets. Where equivalents are shown for temperatures other than the test temperatures, the rate of change of full drive current for a constant disturb ratio of 0.61 is used to calculate the currents required to drive the core.

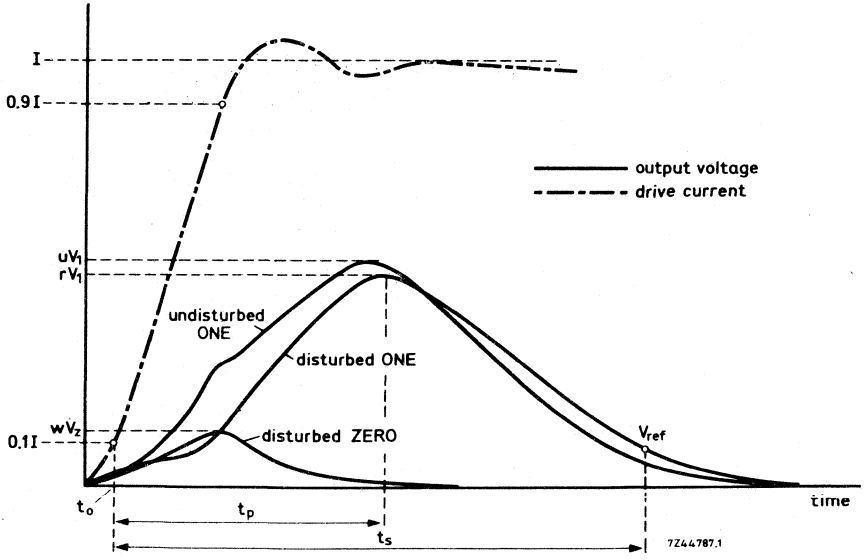
Pulse Sequence

Cores are measured while being subjected to a sequence of pulses designed to cycle the core through a number of states.
The following indicates a typical pulse train used for core measurement:



The pulse repetition frequency is 30 **kHz**. The values of the rV_1 and wV_z response voltages are read after 32 partial disturb pulses, to make sure that the remanent flux density has reached its lowest value.

RESPONSES



System of symbols for core response voltage

The response voltages induced in the sense circuit coupled to the core are measured with the sense circuit terminated in a specified resistance.

Symbols for the various response voltages are built up of the letter V, together with pre-subscripts and post-subscripts. Unless otherwise stated, the peak value of the response is indicated by this symbol.

Post-subscripts

The post-subscripts indicate the type of read pulse (either partial or full) giving rise to the response voltage and also the polarity of the last full-pulse preceding the read pulse, i.e. read or write polarity.

When the response is caused by a full read pulse, the post subscript is:

1 when the last full pulse preceding this was a write pulse (i.e. the core had been storing "one").

z when the last full pulse preceding this was a read pulse (i.e. the core had been storing "zero").

When the response is caused by a partial read pulse the post subscript is:

p1 when the last full pulse preceding this was a write pulse (i.e. the core had been storing "one").

pz when the last full pulse preceding this was a read pulse (i.e. the core had been storing "zero").

Pre-scripts:

The pre-scripts indicate the partial pulses applied to the core between the read pulse at which the response is observed, and the last full pulse applied before that read pulse. These are:

u when there have been no partial pulses (i.e. the core is undisturbed).

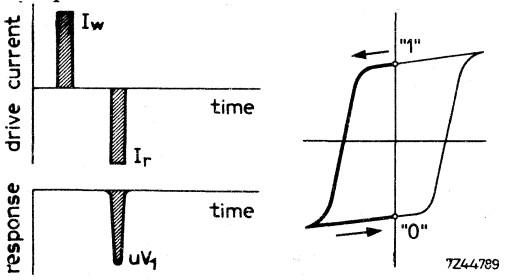
r when there have been one or more partial read pulses.

w when there have been one or more partial write pulses.

Response voltages

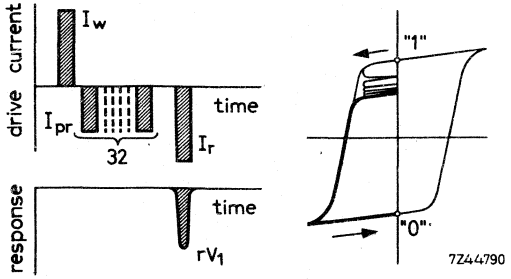
The following are the principal response voltages, which are used in Memory Core data sheets:

uV_1 Undisturbed "One"



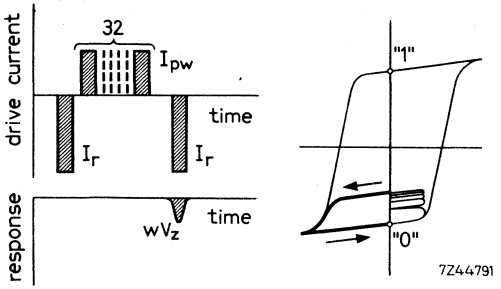
The peak value of the response voltage, obtained at a full read pulse, preceded by a full write pulse.

rV_1 Read disturbed, Fully selected, "One"



The peak value of the response voltage, obtained at a full read pulse, preceded by a full write pulse followed by a number of partial read pulses.

$^{\prime}wV_z$ Write disturbed, Fully selected, "Zero"



The peak value of the response voltage, obtained at a full read pulse, preceded by a full read pulse followed by a number of partial write pulses.

$UR = uV_1 - rV_1$

The difference between the value of uV_1 and rV_1.
This value is a measure for the rectangularity of the hysteresis loop.

Response Times

The following times are used in Memory Core data sheets to describe core responses.

t_o Time Origin. The time when the leading edge of the current pulse reaches 10% of the amplitude of the current pulse. The time origin is the point from which the following response times are measured.

t_p Peak Time. The time interval between the time origin, t_o, and the time at which (rV_1) attains its peak amplitude.

t_s Switching Time. The time interval between the time origin, t_o, and the time at which rV_1 falls to V_{ref} for the last time, ignoring any trailing edge transient.

Notes When it is necessary to refer to the Peak Time or Switching Time of a response voltage other than the rV_1 characteristic, the symbol t_p or t_s may be used, qualified with a symbol in parenthesis to indicate to which response voltage it applies (e.g. t_p (uV_1); t_s (wV_z)).

"V_{ref}" should normally be equal to 0.1 rV_1. Because it is impractical to measure rV_1 of each core of a series of cores exactly and then to adjust for 0.1 rV_1 at each core again, t_s is measured with respect to V_{ref}.

CORE DIMENSIONS

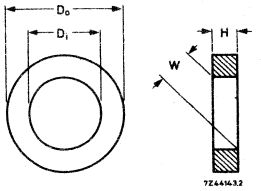
In the data sheets the following dimensions are given (see figure) :

D_o = outer diameter

D_i = inner diameter

H = height

$W = \frac{D_i - H}{\sqrt{2}}$ = wiring passage under 45°



NOMINAL OPERATING CONDITIONS AND TYPICAL RESPONSE CHARACTERISTICS

On each data sheet nominal operating conditions are stated in order to compare one core type with another. These conditions are nominal in as much as, although practical, they will not necessarily be the optimum under any particular set of circumstances.
Typical response characteristics obtained under these nominal operating conditions can be obtained from the data.

QUICK REFERENCE DATA

The data sheets contain the following quick reference data on the front page :

Switching time, this is the switching time at nominal operating conditions and $V_{ref} = 0,1\ rV_1$

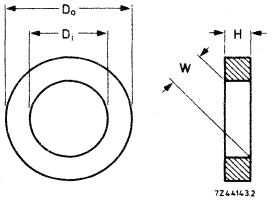
Temperature range, classified as follows : Standard temperature range, up to 55 °C
Medium temperature range, up to 75 °C
Wide temperature range, up to 100 °C

14 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA	
Switching time	0.13 μs
Medium temperature range	

DIMENSIONS

D_o = 0.350 mm (14 mil)
D_i = 0.230 mm (9 mil)
H = 0.075 mm (3 mil)
W = 0.110 mm (4.3 mil)



APPLICATION

This core has been developed for use in a coincident current memory, in particular in $2\frac{1}{2}$ D systems.

ELECTRICAL DATA

nominal operating conditions			typical response values		
T_{amb}	25	°C	uV_1	41	mV
$I_r = I_w = I_{nom}$	855	mA	rV_1	40	mV
D.R.	0.50		wV_z	4	mV
t_r (linear)	0.03	μs	t_p	0.07	μs
t_d	0.16	μs	t_s	0.13	μs

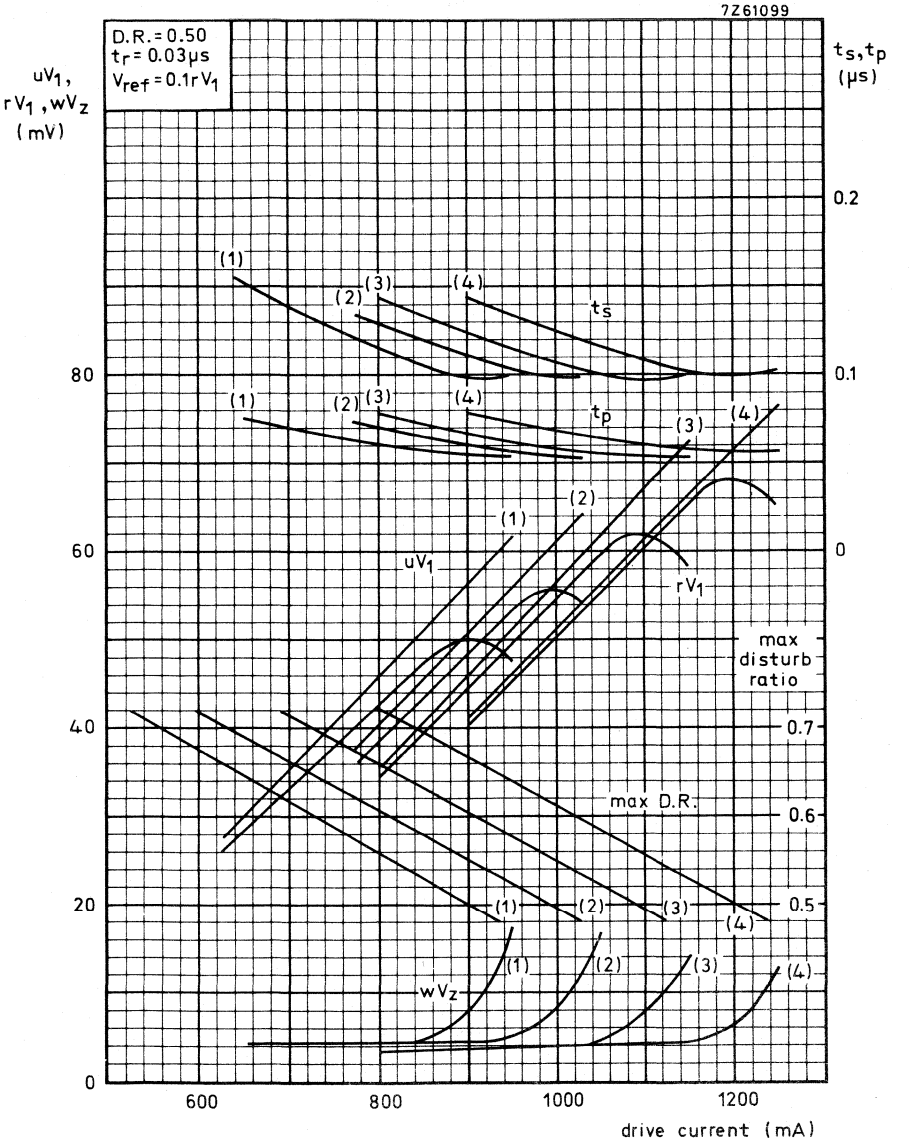
Drift with temperature (average over the range 0 to 75 °C)		
Rate of change of full drive current for constant uV_1	1.9	mA/°C
Rate of change of full drive current at break point and D.R. = 0.61	3.9	mA/°C
Rate of change of uV_1 for constant drive current	0.2	mV/°C

TESTS AND REQUIREMENTS

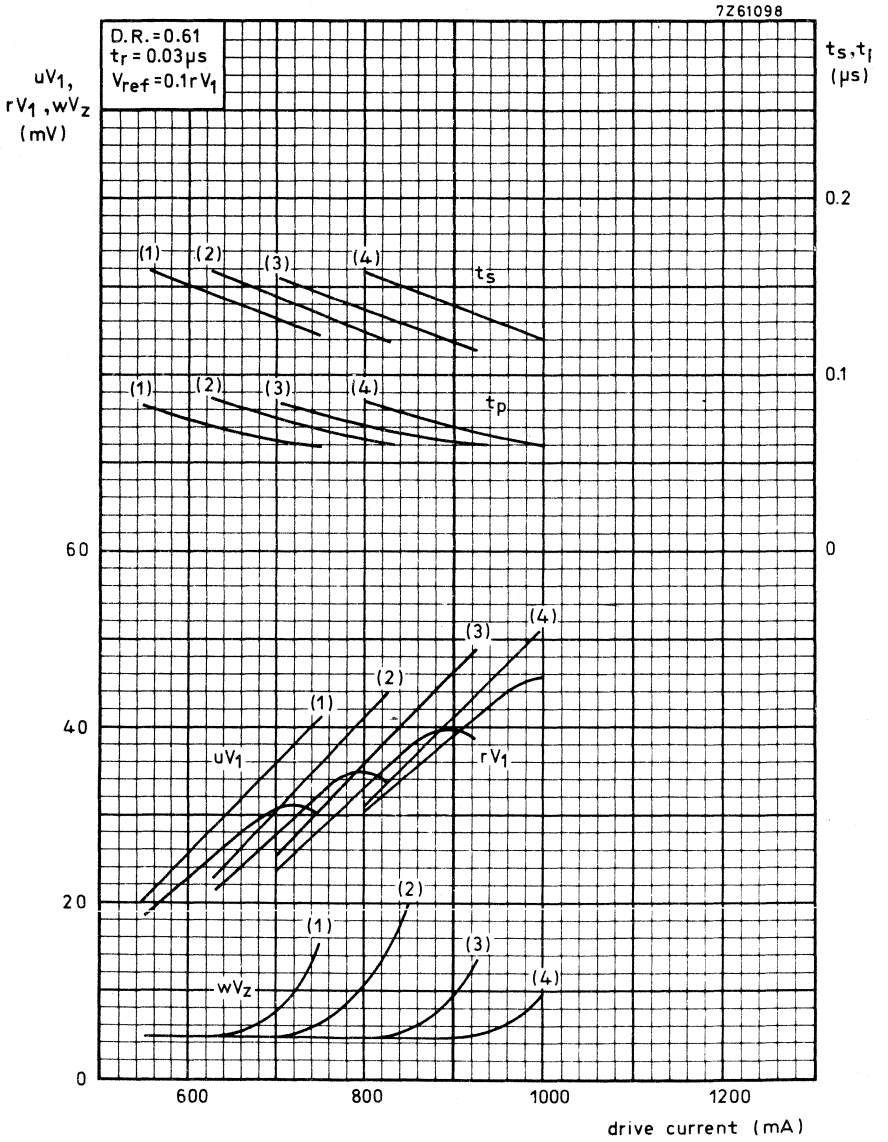
test conditions			equivalent at	
T_{amb}	75	°C	T_{amb} = 25	°C
$I_r = I_w$	675	mA	770	mA
$I_{pr} = I_{pw}$	412	mA	470	mA
D.R.	0.61		0.61	
Number of disturb pulses	32		32	
t_r (linear)	0.03	µs	0.03	µs
t_d	0.30	µs	0.30	µs
V_{ref}	10	mV	10	mV

acceptance limits at test conditions				
rV_1	29 ± 4	mV	30 ± 5	mV
wV_z	≤ 8	mV	≤ 7	mV
UR	≤ 5.5	mV	≤ 4.5	mV
t_p	0.069 ± 0.011	µs	0.072 ± 0.012	µs
t_s	0.110 ± 0.014	µs	0.113 ± 0.015	µs

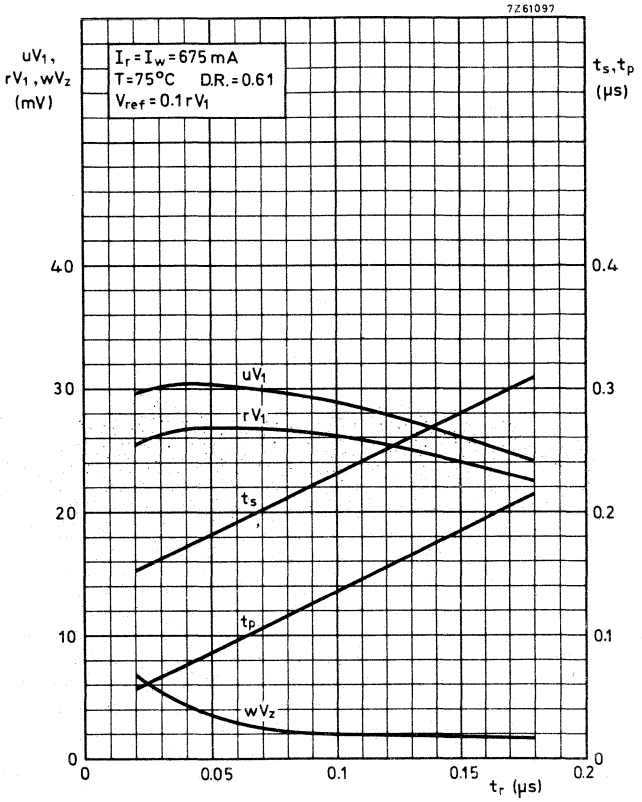
Typical core performance as a function of drive current at different temperatures and DR = 0.50.
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



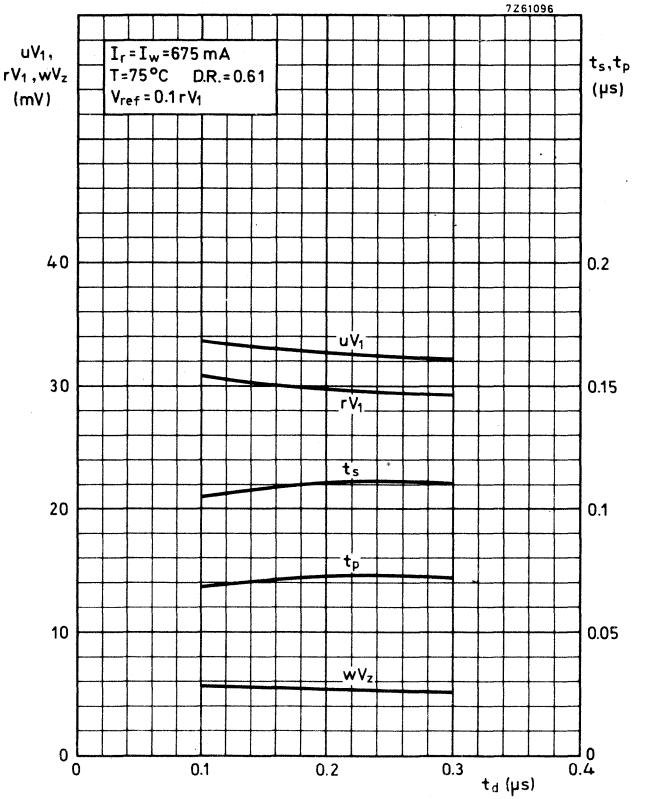
Typical core performance as a function of drive current at different temperatures and DR = 0.61.
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



Typical core performance as a function of current pulse rise time.



Typical core performance as a function of current pulse duration.

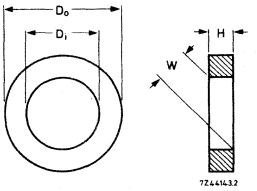


18 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA	
Switching time	0,240 μs
Medium temperature range	

DIMENSIONS

D_o = 0,450 mm (17,6 mil)
D_i = 0,285 mm (11,2 mil)
H = 0,110 mm (4,3 mil)
W = 0,124 mm (4,8 mil)



APPLICATION

This core has been developed for use in a coincident current memory, in particular in 3D systems.

ELECTRICAL DATA

nominal operating conditions	
T_{amb}	25 °C
$I_r = I_w = I_{nom}$	555 mA
D.R.	0,50
t_r (linear)	0,05 μs
t_d	0,3 μs

typical response values	
uV_1	45 mV
rV_1	44 mV
wV_z	5 mV
t_p	0,120 μs
t_s	0,240 μs

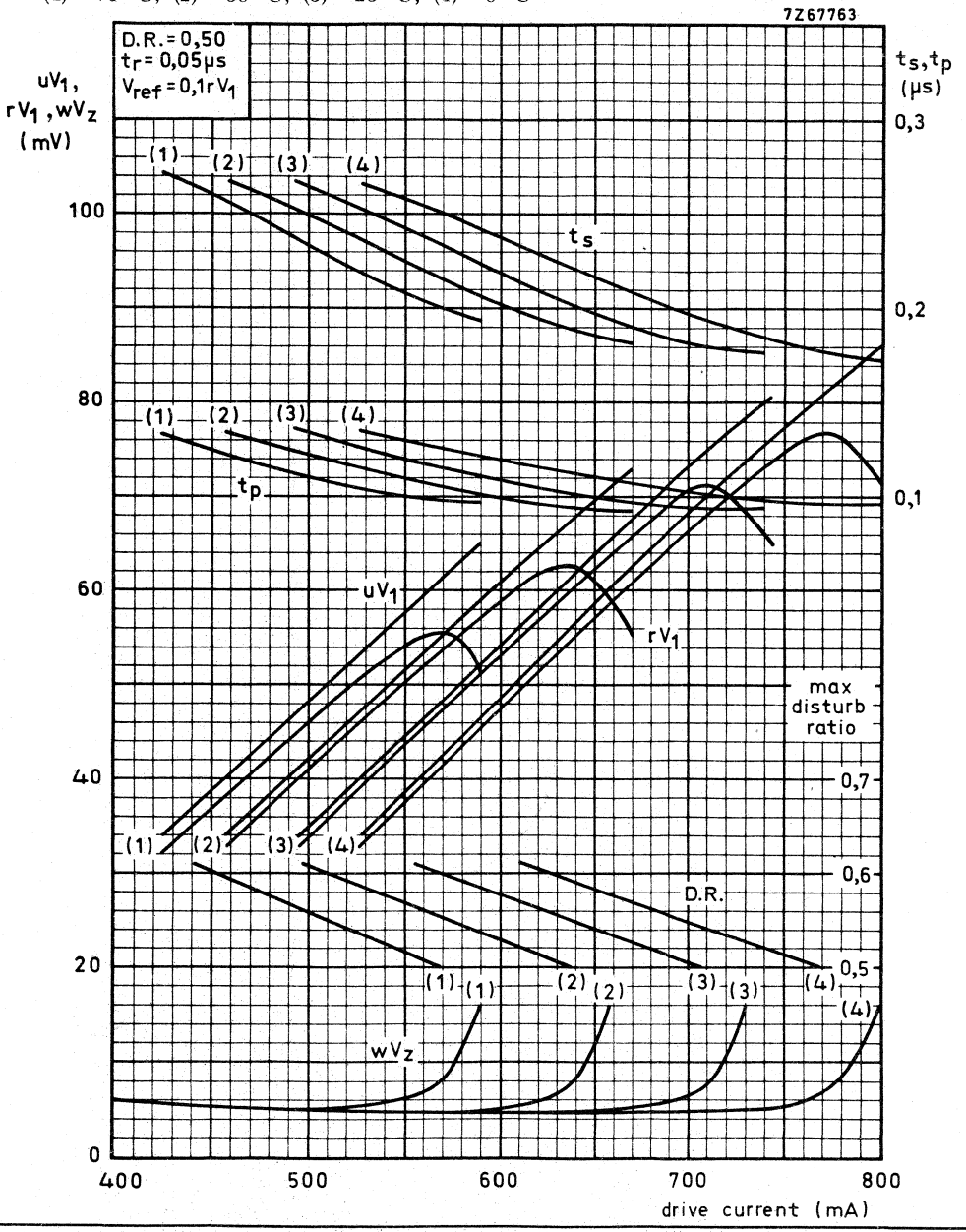
Drift with temperature (average over the range 0 to 75 °C)		
Rate of change of full drive current for constant uV_1	1,3	mA/°C
Rate of change of full drive current at breakpoint and D.R. = 0,61	2,3	mA/°C
Rate of change of uV_1 for constant drive current	0,25	mV/°C

TESTS AND REQUIREMENTS

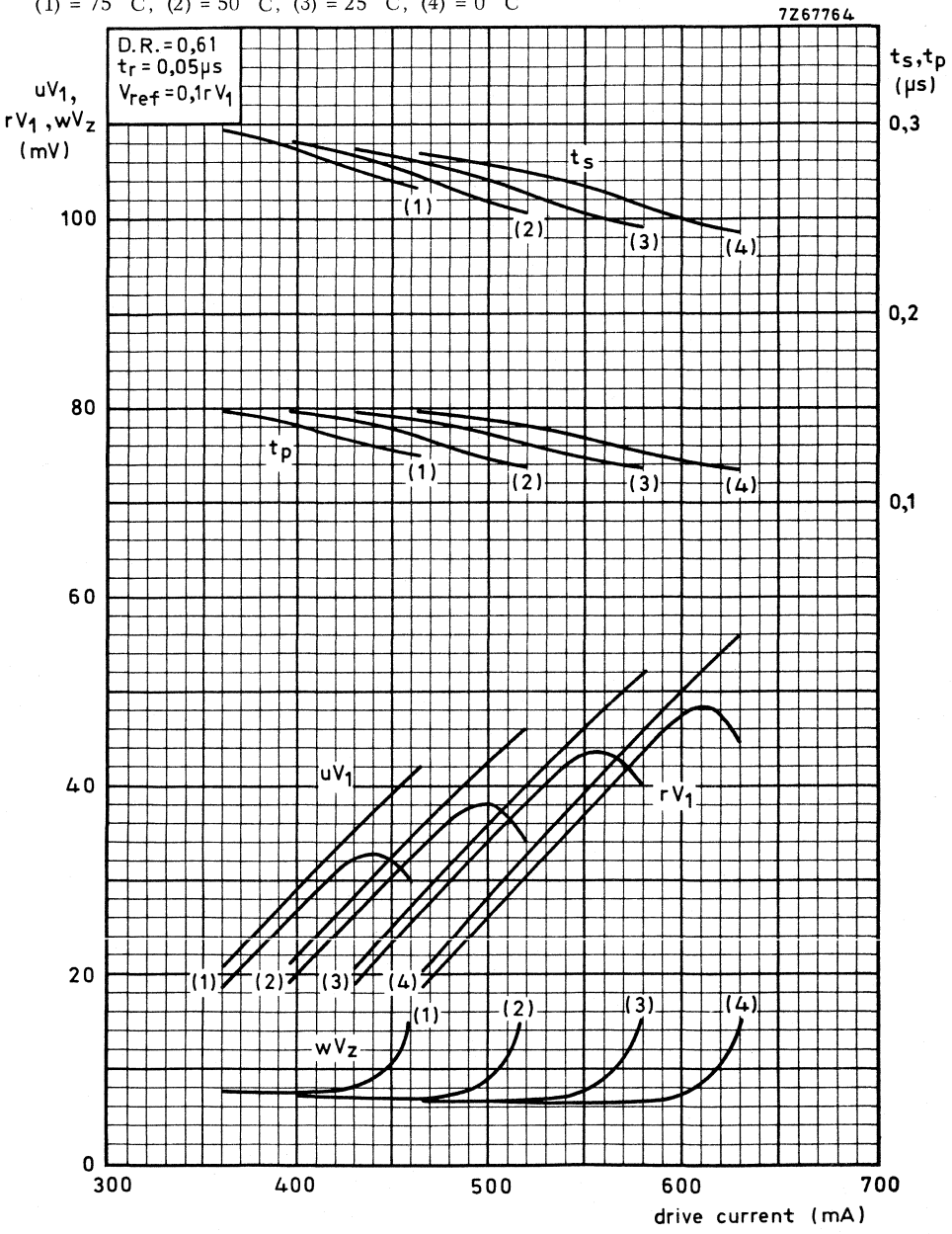
test conditions		equivalent at T_{amb} = 25 °C
T_{amb}	75 °C	
$I_r = I_w$	440 mA	500 mA
$I_{pr} = I_{pw}$	264 mA	305 mA
D.R.	0,60	0,61
Number of disturb pulses	32	32
t_r (linear)	0,05 µs	0,05 µs
t_d	0,50 µs	0,50 µs
V_{ref}	10 mV	10 mV

acceptance limits at test conditions		
rV_1	35 ± 5 mV	36 ± 6 mV
wV_z	≤ 9.5 mV	≤ 9 mV
UR	≤ 5.5 mV	≤ 5 mV
t_p	0,135 ± 0,020 µs	0,135 ± 0,020 µs
t_s	0,220 ± 0,020 µs	0,220 ± 0,020 µs

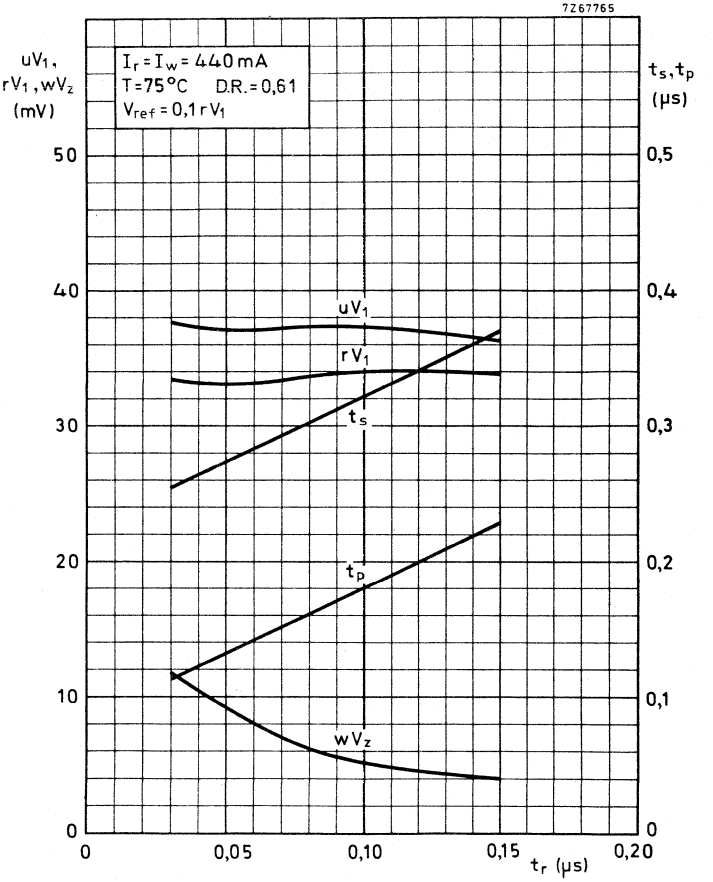
Typical core performance as a function of drive current at different temperatures and D.R. = 0,50
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



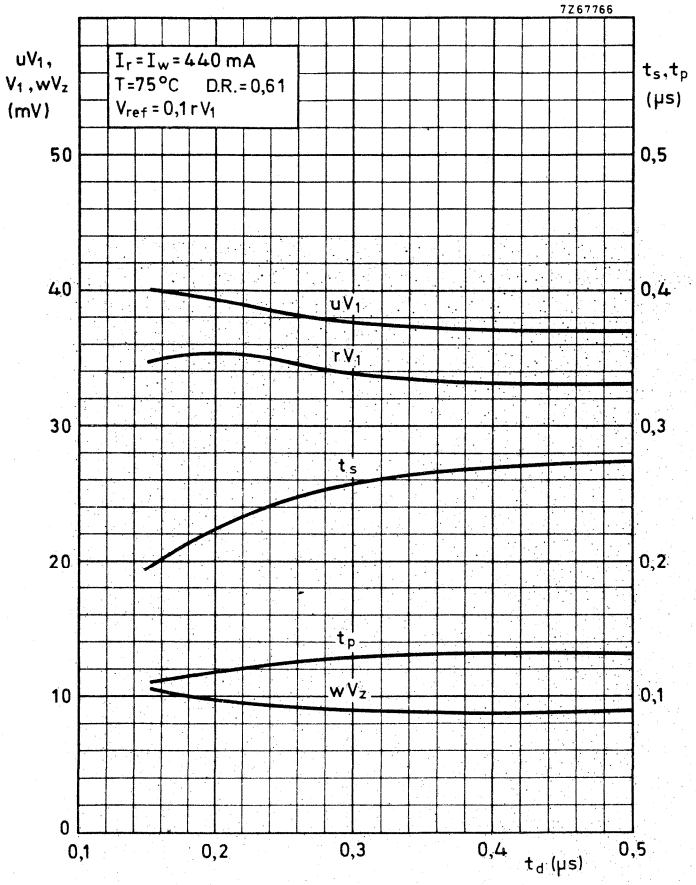
Typical core performance as a function of drive current at different temperatures and D.R. = 0,61
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



Typical core performance as a function of current pulse rise time



Typical core performance as a function of current pulse duration

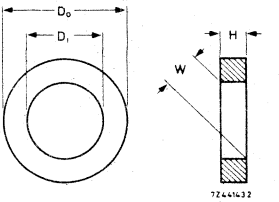


18 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA	
Switching time	0.210 μs
Medium temperature range	

DIMENSIONS

D_o = 0.450 mm (17.6 mil)
D_i = 0.280 mm (11.2 mil)
H = 0.110 mm (4.3 mil)
W = 0.120 mm (4.8 mil)



APPLICATION

This core has been developed for use in a coincident current memory, in particular in 3 D systems.

ELECTRICAL DATA

nominal operating conditions		
T_{amb}	25	°C
$I_r = I_w = I_{nom}$	644	mA
D.R.	0.50	
t_r (linear)	0.05	μs
t_d	0.25	μs

typical response values		
uV_1	55	mV
rV_1	53	mV
wV_z	5	mV
t_p	0.110	μs
t_s	0.210	μs

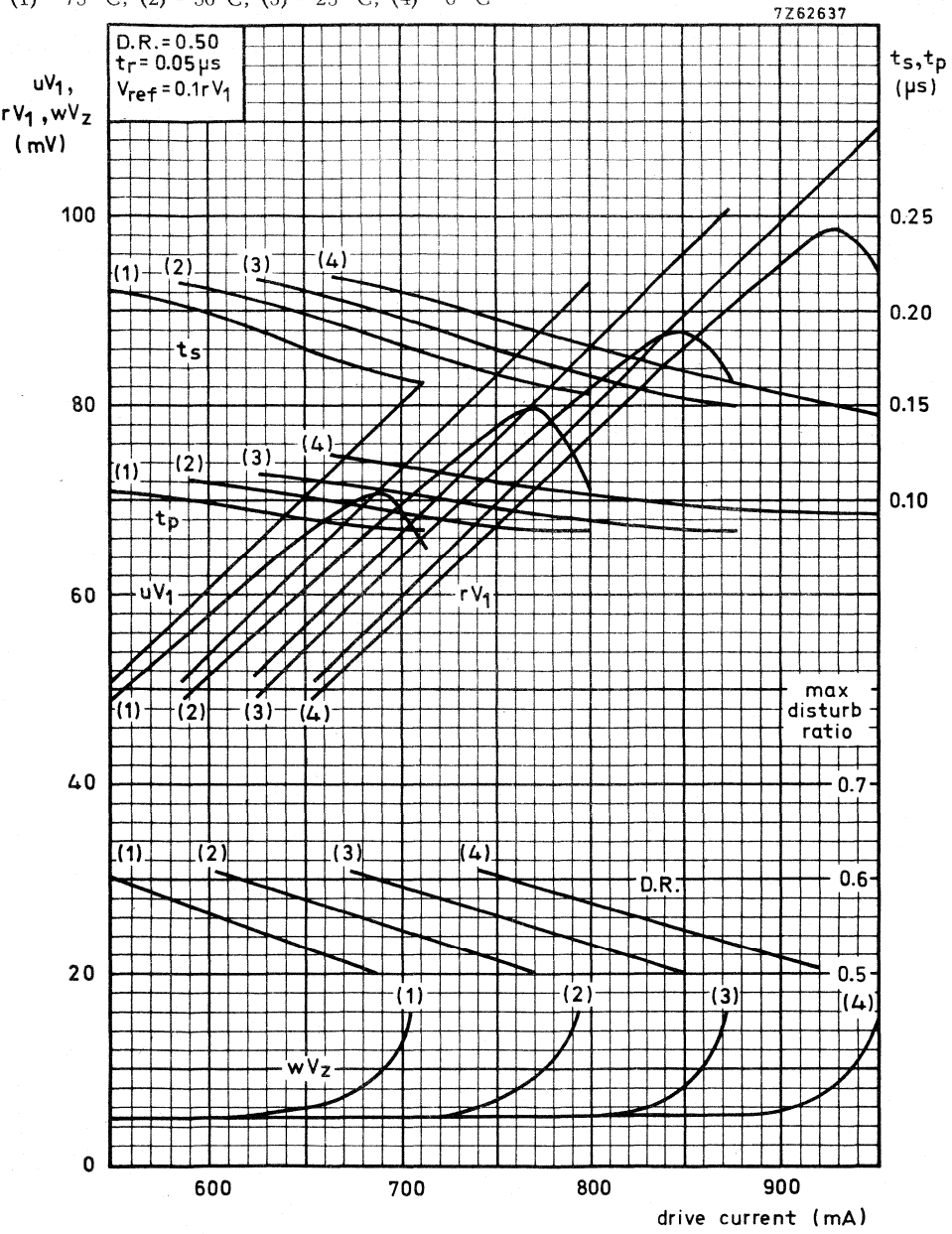
Drift with temperature (average over the range 0 to 75 °C)	
Rate of change of full drive current for constant uV_1	1.4 mA/°C
Rate of change of full drive current at break point and D.R. = 0.61	2.7 mA/°C
Rate of change of uV_1 for constant drive current	0.3 mV/°C

TESTS AND REQUIREMENTS

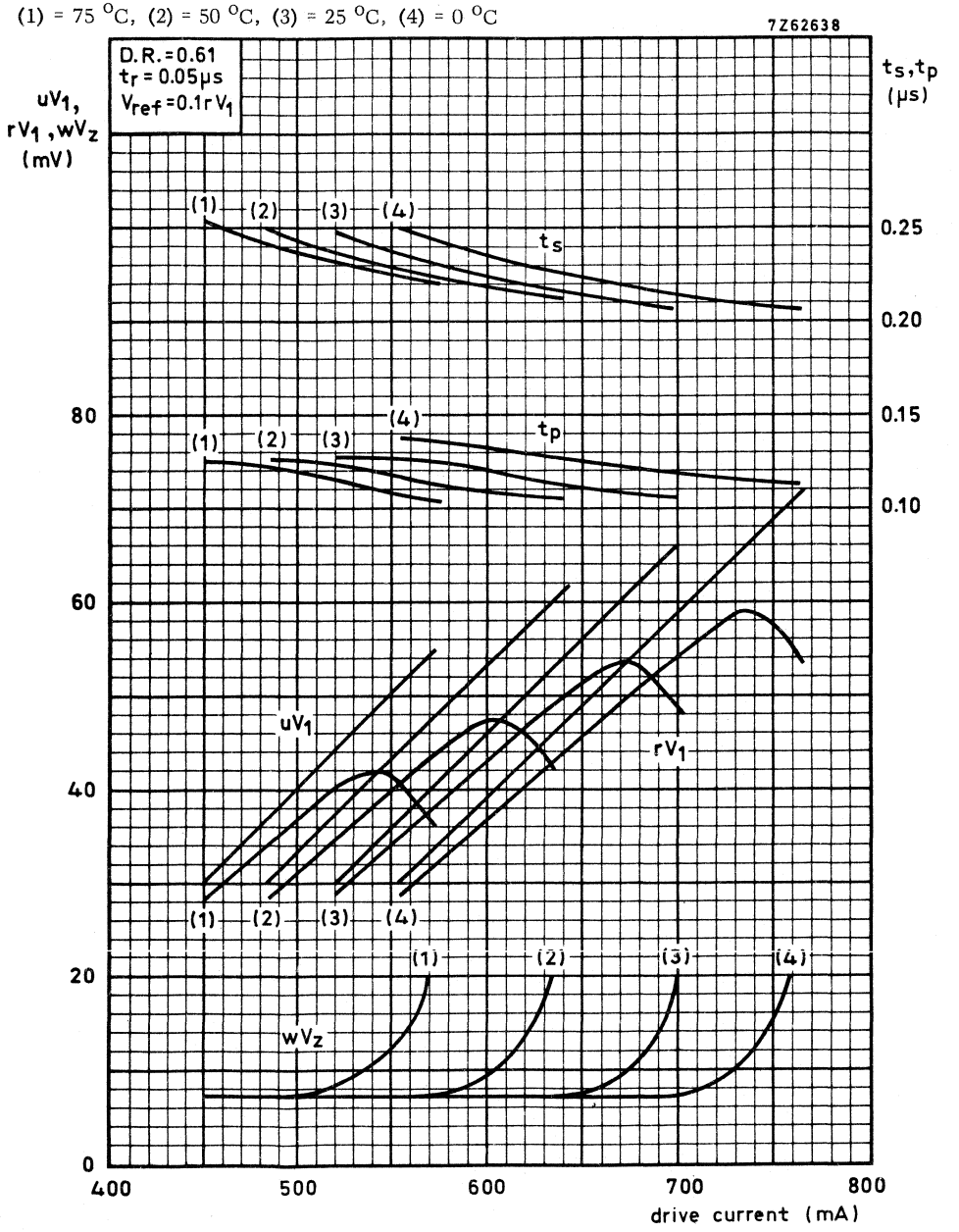
test conditions			equivalent at T_{amb} = 25 °C	
T_{amb}	75	°C		
$I_r = I_w$	510	mA	580	mA
$I_{pr} = I_{pw}$	311	mA	354	mA
D.R.	0.61		0.61	
Number of disturb pulses	32		32	
t_r (linear)	0.05	µs	0.05	µs
t_d	0.3	µs	0.3	µs
V_{ref}	10	mV	10	mV

acceptance limits at test conditions				
rV_1	39 ± 5	mV	39 ± 7	mV
wV_z	≤ 9.5	mV	≤ 9.0	mV
UR	≤ 6	mV	≤ 5.5	mV
t_p	0.120 ± 0.020	µs	0.120 ± 0.020	µs
t_s	0.205 ± 0.020	µs	0.205 ± 0.020	µs

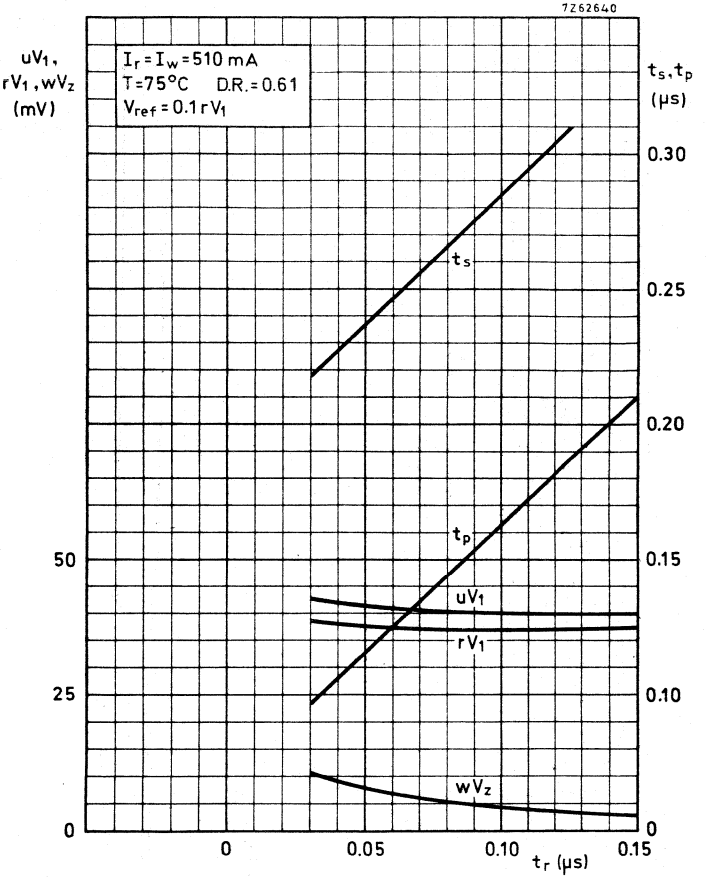
Typical core performance as a function of drive current at different temperatures and DR=0.50
(1) = 75 °C, (2) = 50°C, (3) = 25 °C, (4) = 0 °C



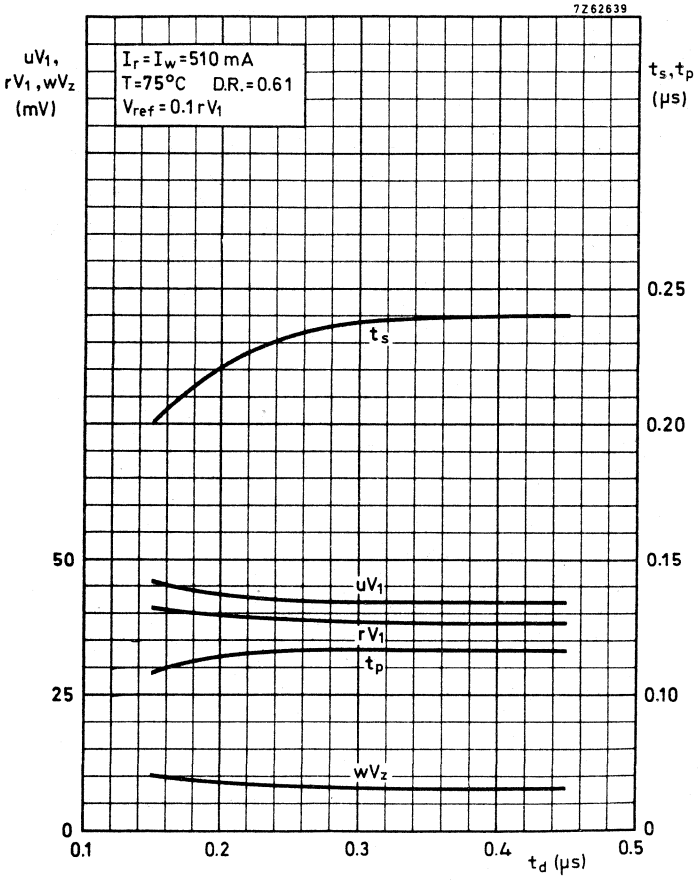
Typical core performance as a function of drive current at different temperatures and DR = 0.61
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



Typical core performance as a function of current pulse rise time.



Typical core performance as a function of current pulse duration.

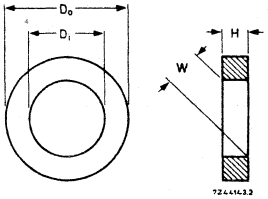


18 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA		
Switching time	0.170	μs
Medium temperature range		

DIMENSIONS

D_o = 0.455 mm (17.8 mil)
D_i = 0.285 mm (11.2 mil)
H = 0.115 mm (4.5 mil)
W = 0.120 mm (4.7 mil)



APPLICATION

This core has been developed for use in a coincident current memory, in particular in 3 D systems.

ELECTRICAL DATA

nominal operating conditions		
T_{amb}	25	°C
$I_r = I_w = I_{nom}$	800	mA
D.R.	0.50	
t_r (linear)	0.05	μs
t_d	0.20	μs

typical response values		
uV_1	66	mV
rV_1	64	mV
wV_z	6	mV
t_p	0.095	μs
t_s	0.170	μs

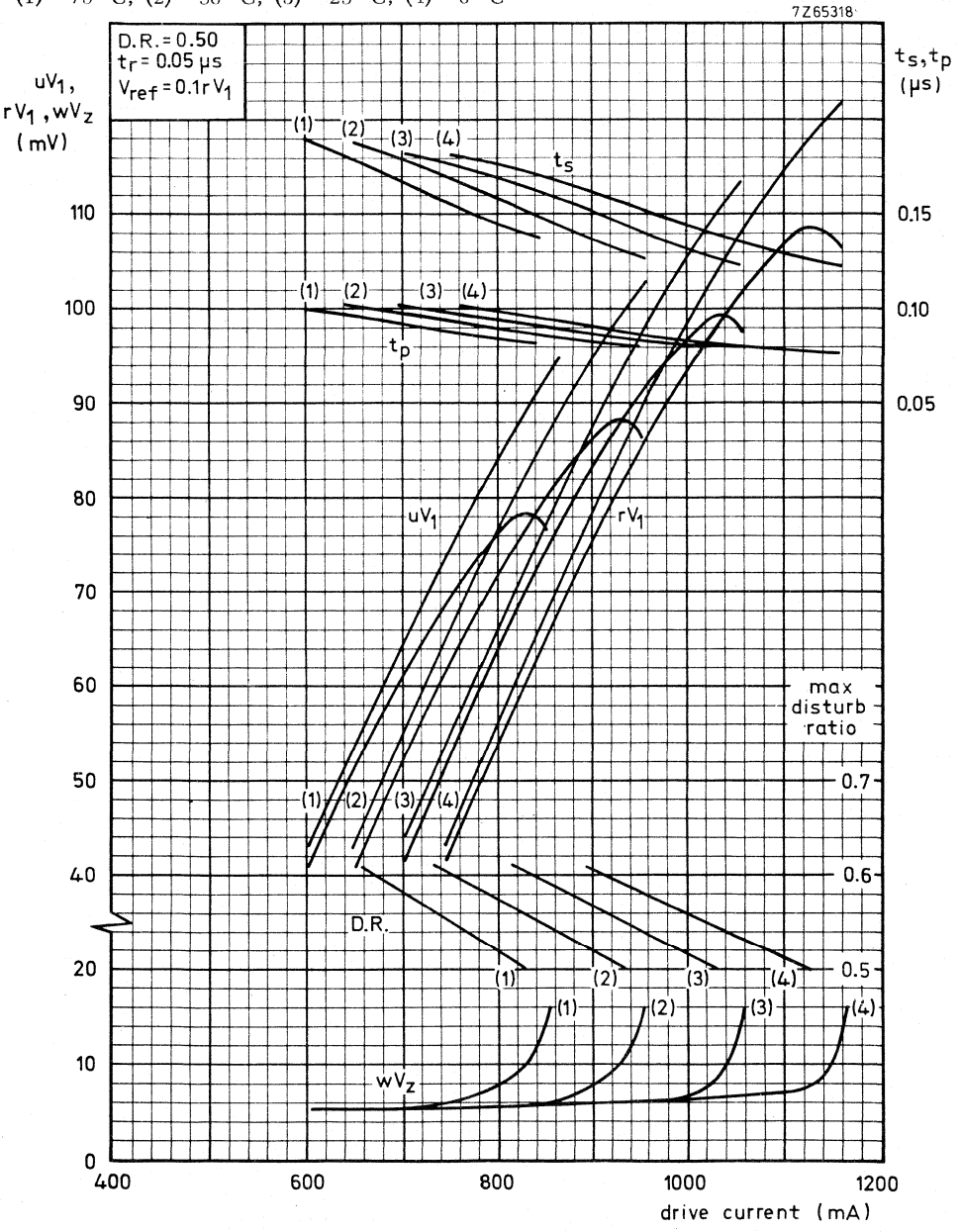
Drift with temperature (average over the range 0 to 75 °C)	
Rate of change of full drive current for constant uV_1	2.0 mA/°C
Rate of change of full drive current at break point and D.R.=0.61	3.1 mA/°C
Rate of change of uV_1 for constant drive current	0.5 mV/°C

TESTS AND REQUIREMENTS

test conditions			equivalent at T_{amb} = 25 °C	
T_{amb}	75	°C		
$I_r = I_w$	620	mA	720	mA
$I_{pr} = I_{pw}$	378	mA	439	mA
D.R.	0.61		0.61	
Number of disturb pulses	32		32	
t_r (linear)	0.05	µs	0.05	µs
t_d	0.30	µs	0.30	µs
V_{ref}	10	mV	10	mV

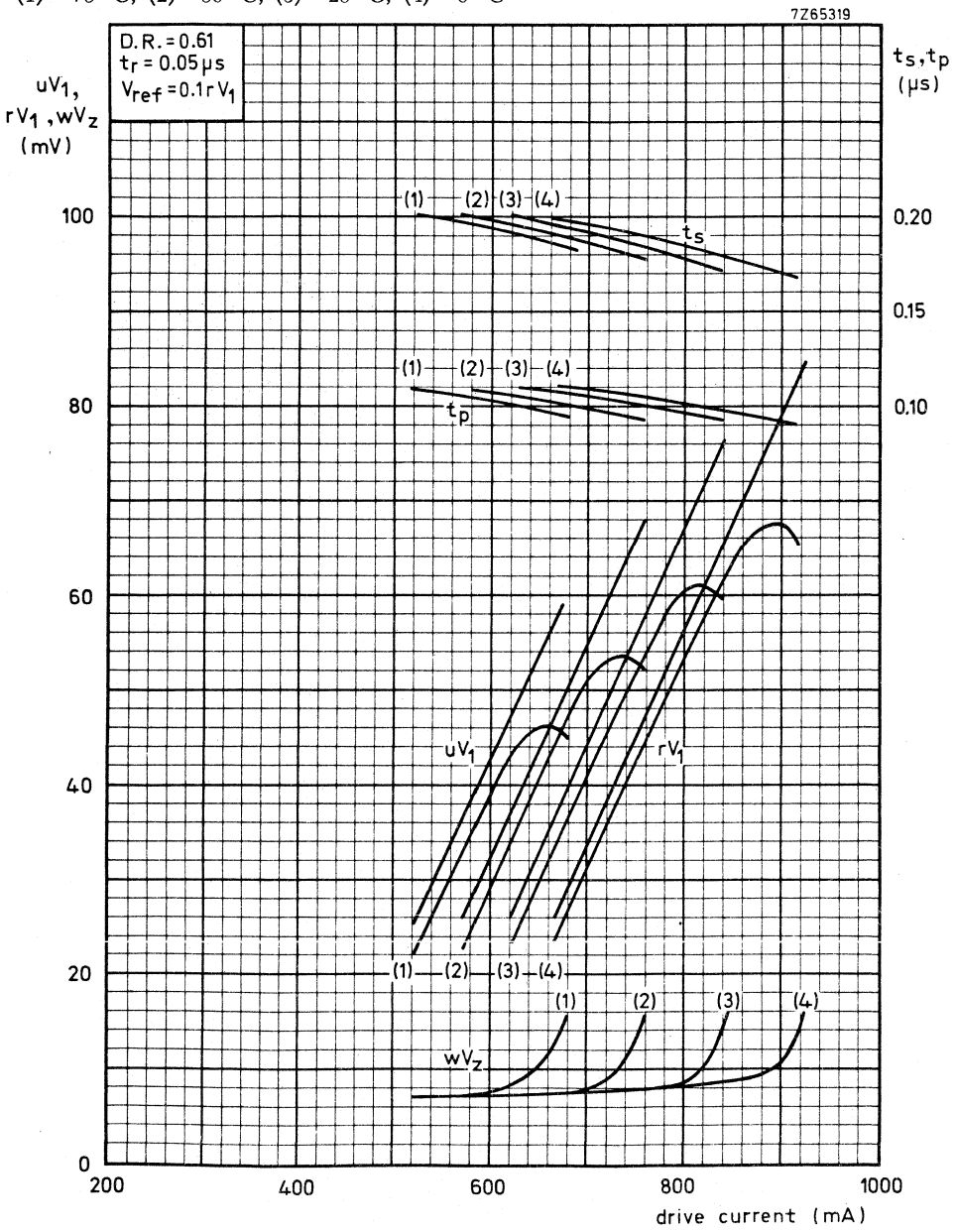
acceptance limits at test conditions				
rV_1	42 ± 5	mV	45 ± 7	mV
wV_z	≤ 12	mV	≤ 11	mV
UR	≤ 7	mV	≤ 6	mV
t_p	0.100 ± 0.020	µs	0.100 ± 0.020	µs
t_s	0.150 - 0.185	µs	0.150 - 0.185	µs

Typical core performance as a function of drive current at different temperatures and DR = 0.50
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C

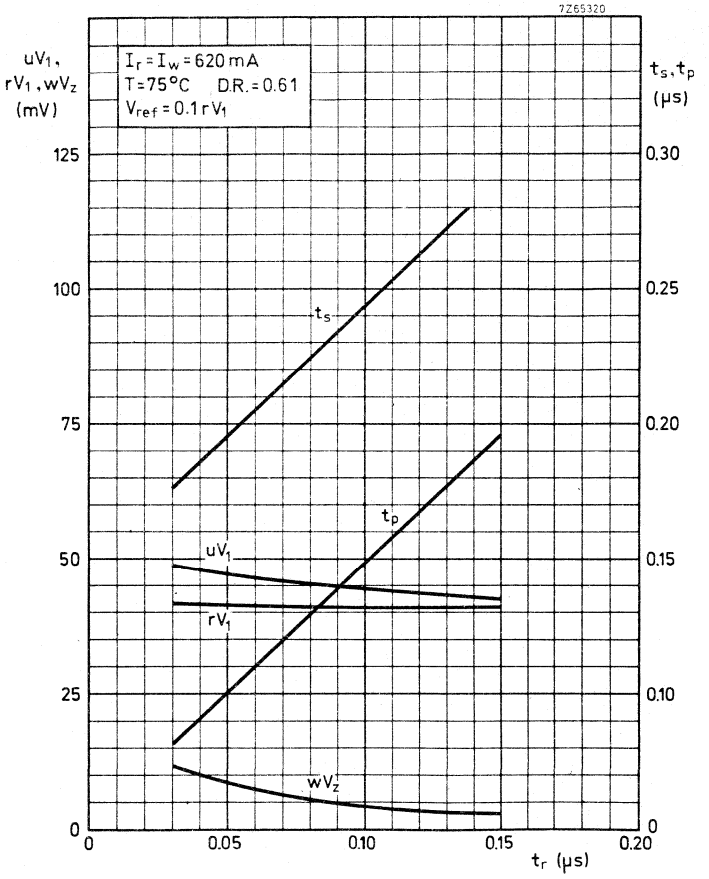


Typical core performance as a function of drive current at different temperatures and DR = 0.61

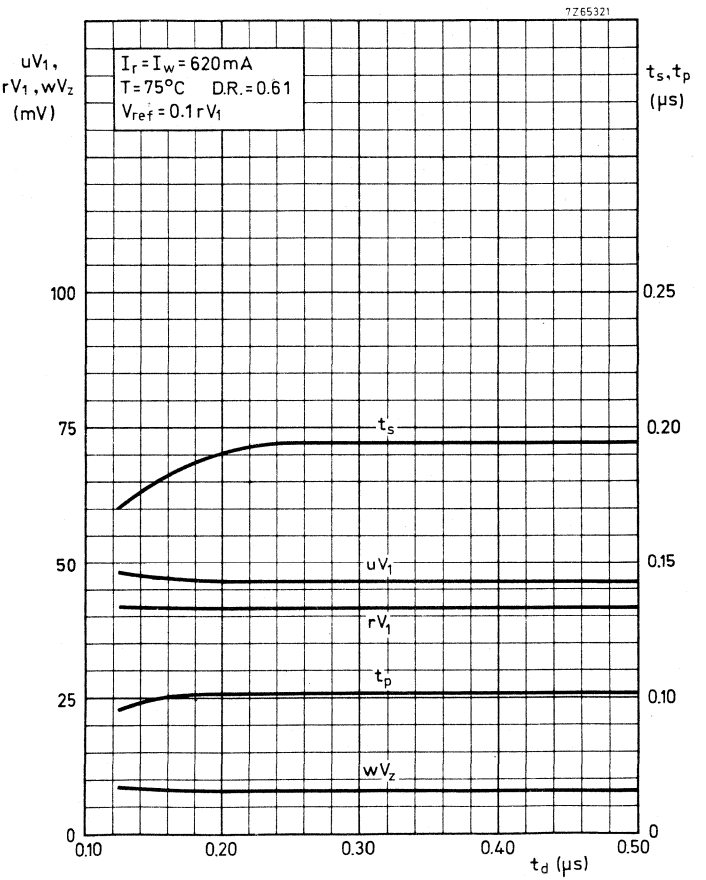
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



Typical core performance as a function of current pulse rise time.



Typical core performance as a function of current pulse duration.

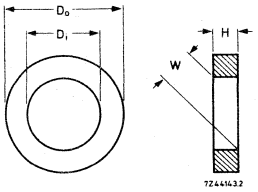


18 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA	
Switching time	0,190 μs
Medium temperature range	

DIMENSIONS

D_o = 0,457 mm (18 mil)
D_i = 0,305 mm (12 mil)
H = 0,105 mm (4,1 mil)
W = 0,143 mm (5,6 mil)



APPLICATION

This core has been developed for use in a coincident current memory, in particular in 3 D systems.

ELECTRICAL DATA

nominal operating conditions	
T_{amb}	25 °C
$I_r = I_w = I_{nom}$	833 mA
D.R.	0,50
t_r (linear)	0,05 μs
t_d	0,30 μs

typical response values	
uV_1	55 mV
rV_1	54 mV
wV_z	4 mV
t_p	0,105 μs
t_s	0,190 μs

Drift with temperature (average over the range 25 to 75 °C)	
Rate of change of full drive current for constant uV_1	2,0 mA/°C
Rate of change of full drive current at break point and D.R. = 0,61	3,5 mA/°C
Rate of change of uV_1 for constant drive current	0,3 mV/°C

TEST AND REQUIREMENTS

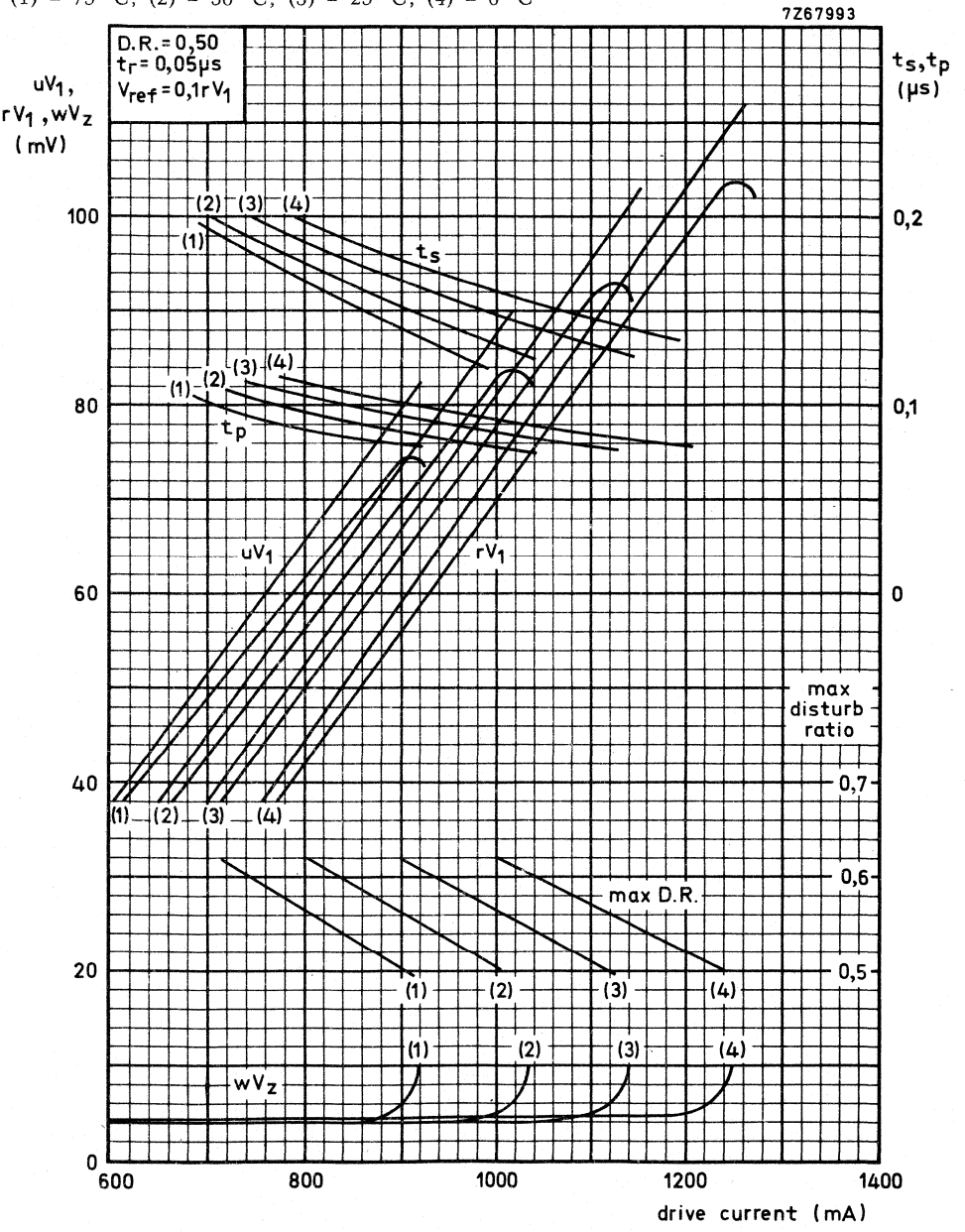
test conditions			equivalent at T_{amb} = 25 °C	
T_{amb}	75	°C		
$I_r = I_w$	650	mA	750	mA
$I_{pr} = I_{pw}$	397	mA	480	mA
D.R.	0,61		0,64	
Number of disturb pulses	32		32	
t_r (linear)	0,05	µs	0,05	µs
t_d	0,30	µs	0,30	µs
V_{ref}	10	mV	10	mV

acceptance limits at test conditions				
rV_1	40 ± 5	mV	42 ± 7	mV
wV_z	≤ 9	mV	≤ 9	mV
UR	≤ 7	mV	≤ 7	mV
t_p	0,115 ± 0,015	µs	0,115 ± 0,015	µs
t_s	0,180 ± 0,020	µs	0,180 ± 0,020	µs

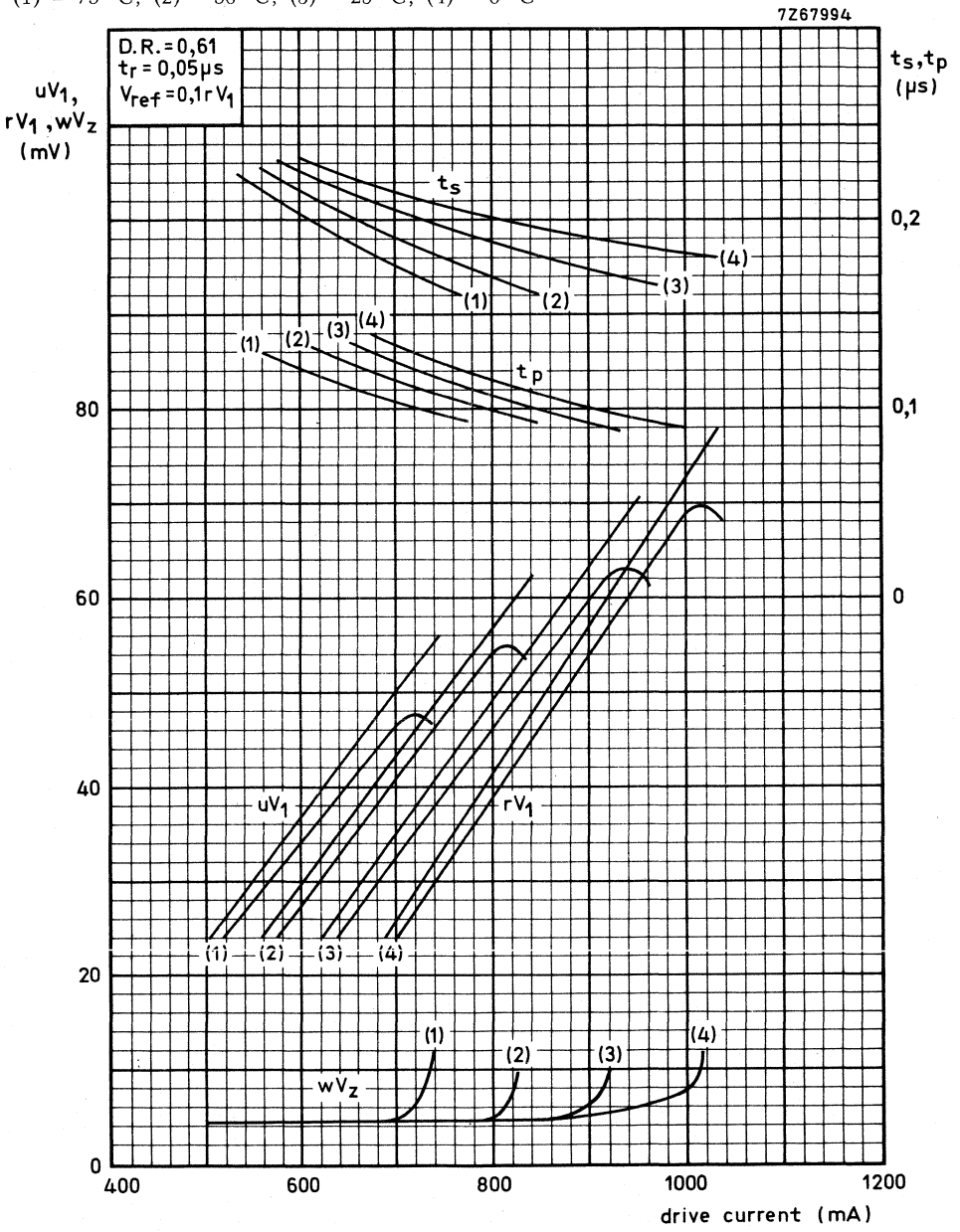
ADDITIONAL DATA

Breakdown voltage	1000 V approximately
Diametric breaking force	min. 0,4 N
Weight per 100 cores	4,2 mg

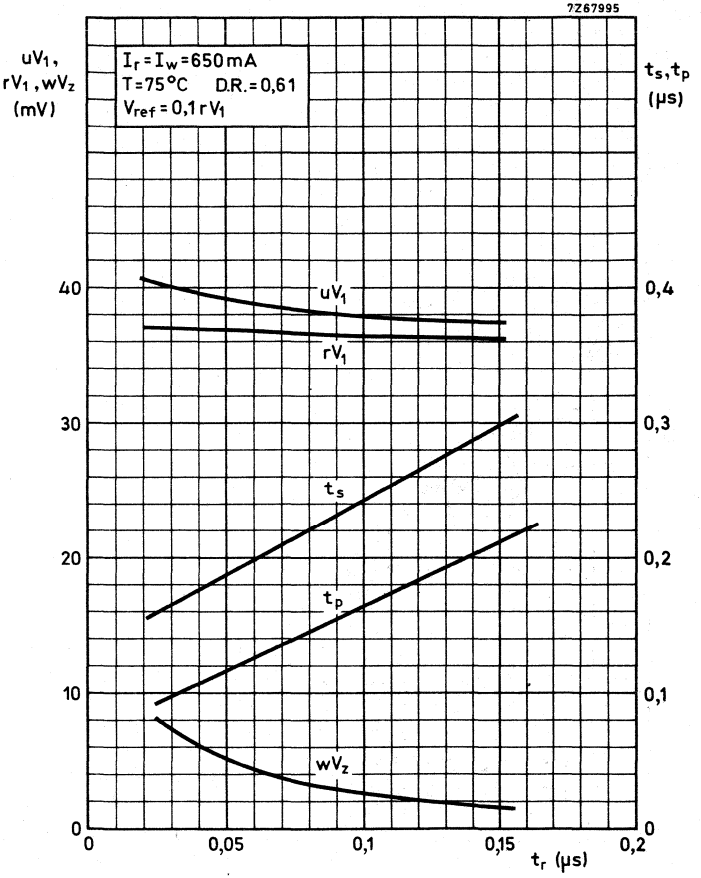
Typical core performance as a function of drive current at different temperatures and D.R. = 0,50
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



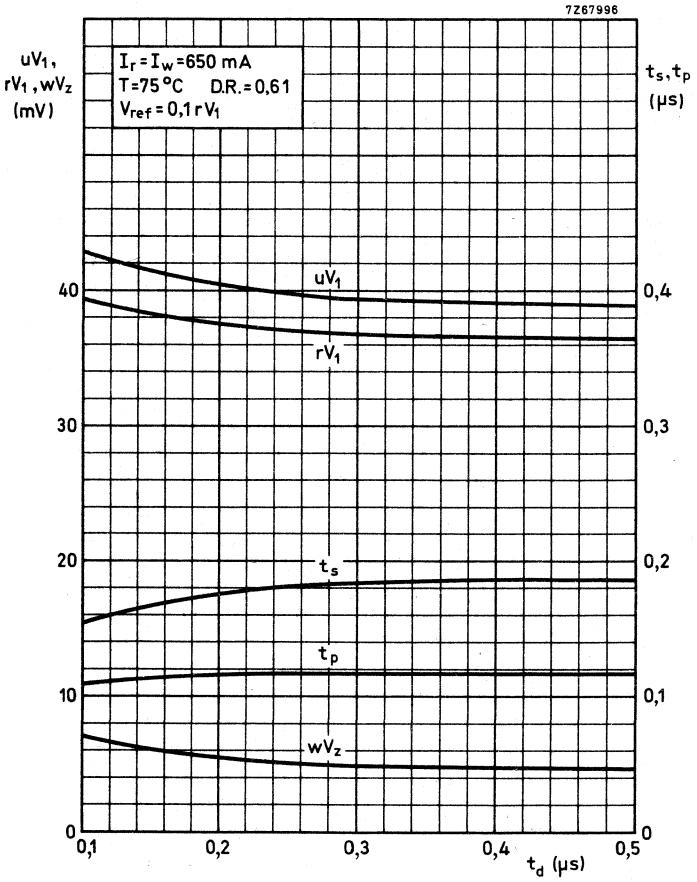
Typical core performance as a function of drive current at different temperatures and D.R. = 0,61
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



Typical core performance as a function of current pulse rise time.



Typical core performance as a function of current pulse duration.

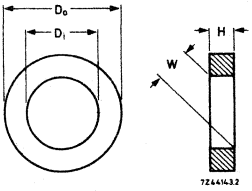


18 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA	
Switching time	0.175 μs
Standard temperature range	

DIMENSIONS

D_o = 0.440 mm (17.2 mil)
D_i = 0.275 mm (10.8 mil)
H = 0.110 mm (4.3 mil)
W = 0.117 mm (4.6 mil)



APPLICATION

This core has been developed for use in a coincident current memory, in particular in $2\frac{1}{2}$ D systems.

ELECTRICAL DATA

nominal operating conditions		
T_{amb}	25	°C
$I_w = I_r = I_{nom}$	825	mA
DR	0.50	
t_r (linear)	0.05	μs
t_d	0.21	μs

typical response values		
T_{amb}	25	°C
uV_1	53	mV
rV_1	52	mV
wV_z	5	mV
t_p	0.095	μs
t_s	0.175	μs

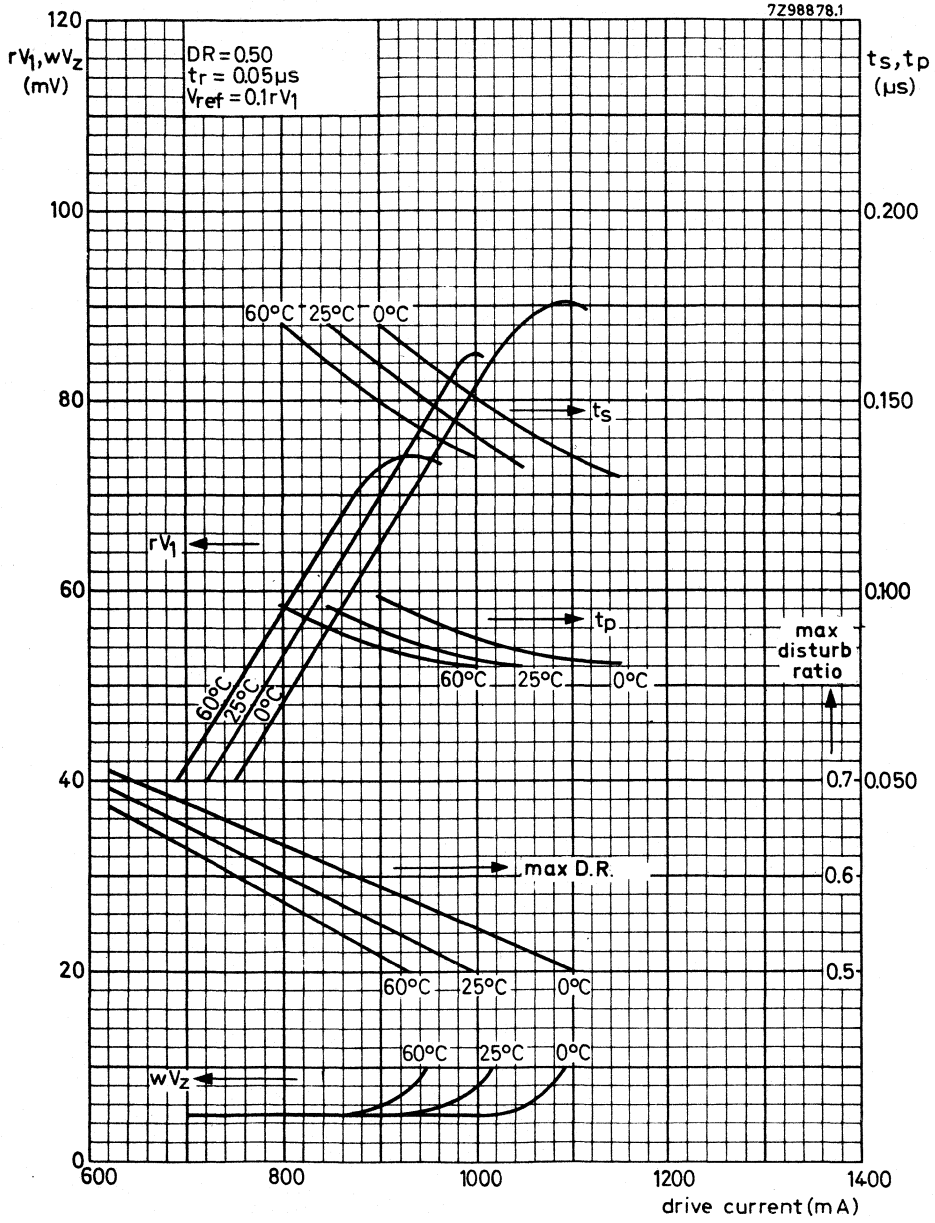
Drift with temperature (average over the range 10 to 55 °C)	
Rate of change of full drive current for constant uV_1	1.3 mA/°C
Rate of change of full drive current at break point and D.R. = 0.61	2.1 mA/°C
Rate of change of uV_1 for constant drive current	0.2 mV/°C

TESTS AND REQUIREMENTS

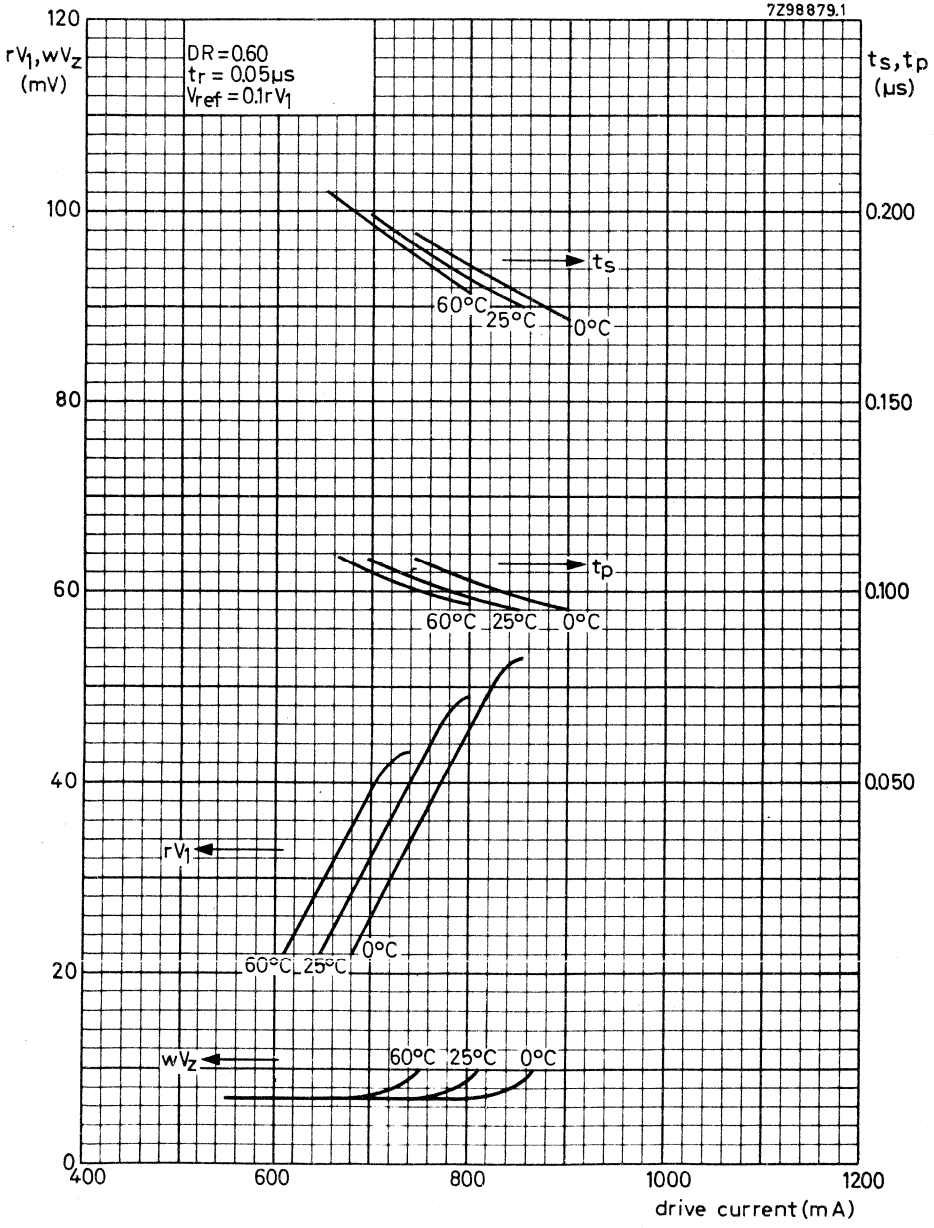
test conditions			
T_{amb}	25	60	°C
$I_w = I_r = I_{nom} - 9\%$	750	700	mA
$I_{pw} = I_{pr} = 0.5\, I_{nom} + 9\%$	450	420	mA
DR	0.60	0.60	
t_r (linear)	0.05	0.05	µs
t_d	0.30	0.30	µs
V_{ref}	10	10	mV

guaranteed values at specified test conditions			
T_{amb}	25	60	°C
rV_1	33-45	33-43	mV
wV_z	≤ 9.5	≤ 10.5	mV
UR	≤ 5.5	≤ 6.5	mV
t_p	0.085-0.115		µs
t_s	0.140-0.175		µs

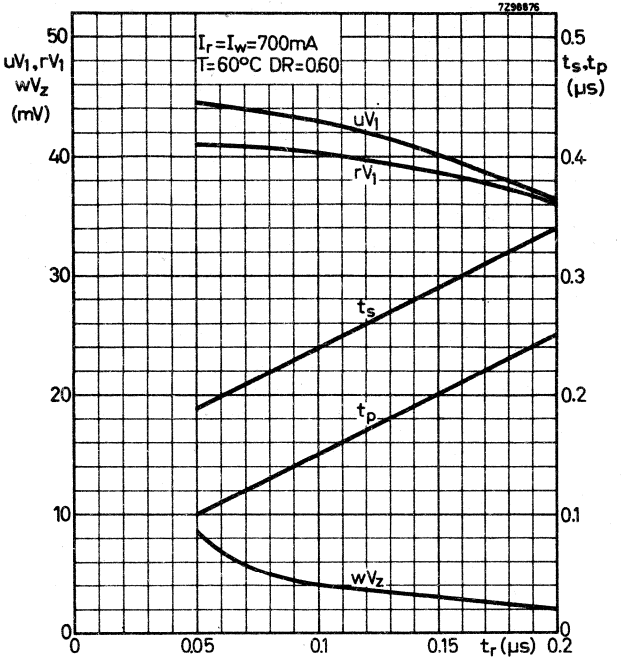
Typical core performance as a function of drive current at different temperatures and D.R. = 0, 50



Typical core performance as a function of drive current at different temperatures and DR = 0.60



Typical core performance as a function of current pulse rise time.

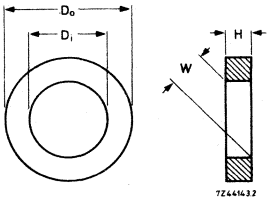


20 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA	
Switching time	0.220 μs
Standard temperature range	

DIMENSIONS

D_o = 0.525 mm (20.7 mil)
D_i = 0.320 mm (12.9 mil)
H = 0.128 mm (5.0 mil)
W = 0.136 mm (5.6 mil)



APPLICATION

This core has been developed for use in a coincident current memory, in particular in 3 D systems.

ELECTRICAL DATA

nominal operating conditions		
T_{amb}	25	°C
$I_r = I_w = I_{nom}$	710	mA
D.R.	0.50	
t_r (linear)	0.05	μs
t_d	0.26	μs

typical response values		
uV_1	66	mV
rV_1	63	mV
wV_z	5	mV
t_p	0.110	μs
t_s	0.220	μs

Drift with temperature (average over the range 10 to 55 °C)		
Rate of change of full drive current for constant uV_1	2.7	mA/°C
Rate of change of full drive current at break point and D.R. = 0.61	4.3	mA/°C
Rate of change of uV_1 for constant drive current	0.53	mV/°C

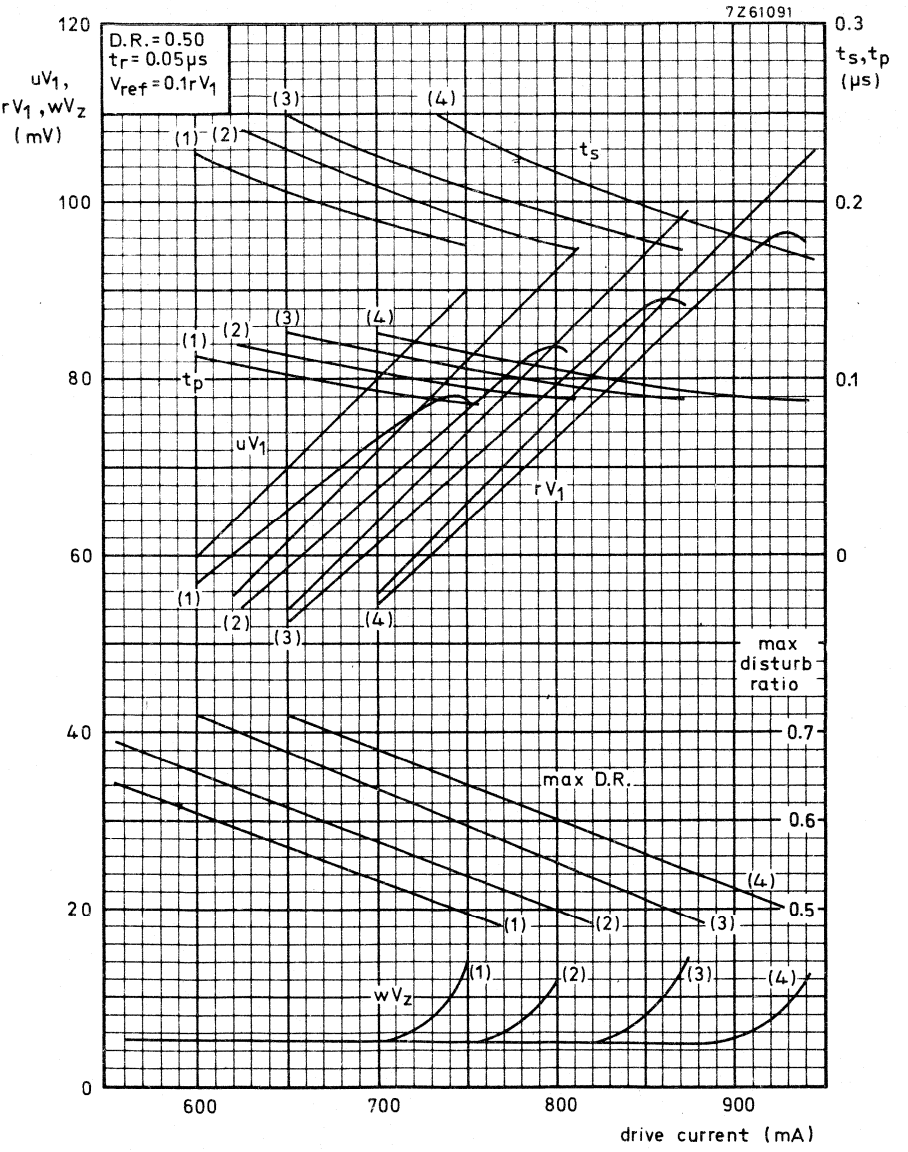
TESTS AND REQUIREMENTS

test conditions			
T_{amb}	45	25	°C
$I_r = I_w$	600	640	mA
$I_{pr} = I_{pw}$	360	385	mA
D.R.	0.60	0.60	
Number of disturb pulses	32	32	
t_r (linear)	0.05	0.05	µs
t_d	0.30	0.30	µs
V_{ref}	5	5	mV

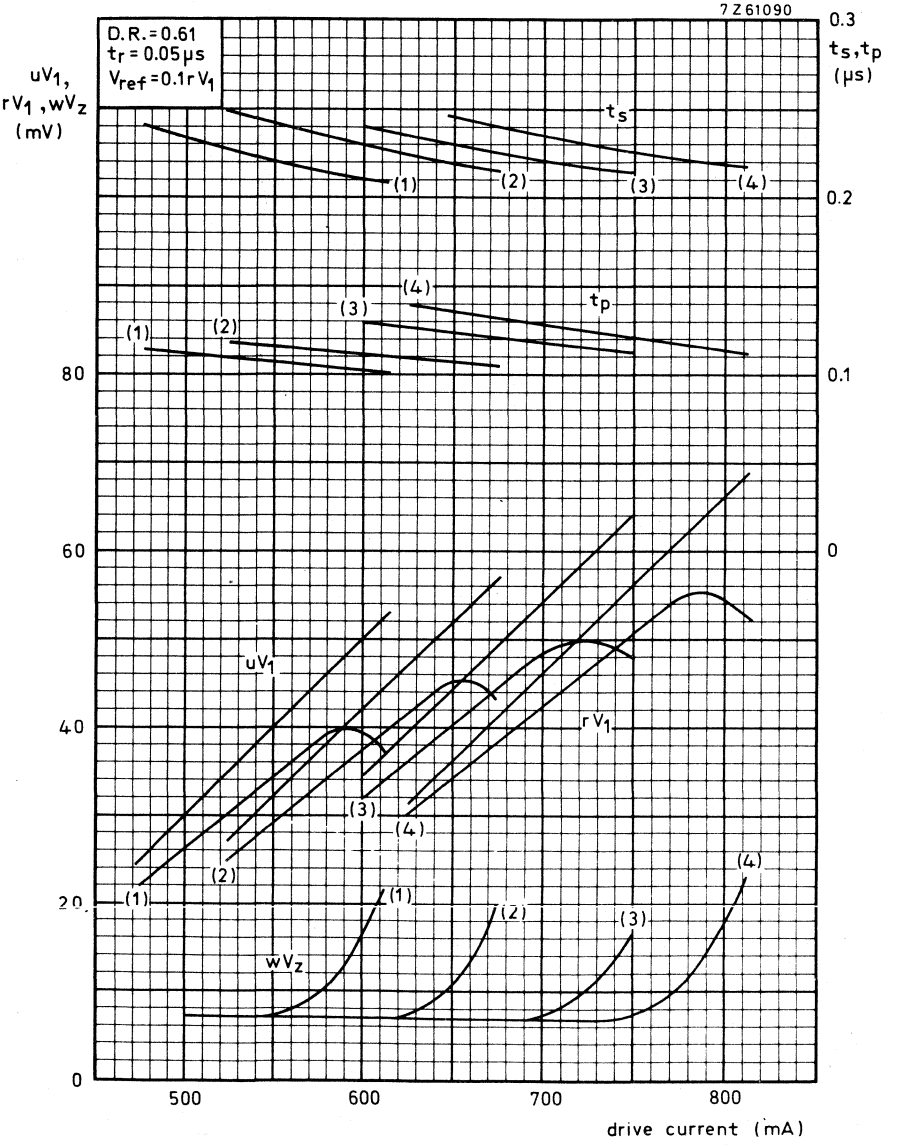
acceptance limits at test conditions			
rV_1	42 ± 5	≥ 31 *)	mV
wV_z	≤ 10.5	≤ 10.5	mV
UR	≤ 6	≤ 6	mV
t_p	0.13 ± 0.02	0.13 ± 0.02	µs
t_s	0.230 ± 0.020	0.225 ± 0.025	µs

*) measured at 0.13 µs

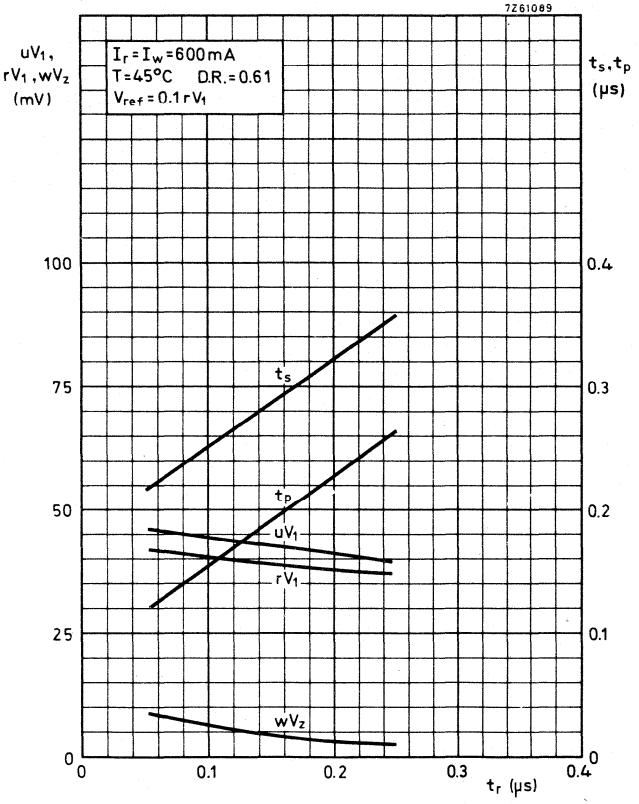
Typical core performance as a function of drive current at different temperatures and DR = 0.50.
(1) = 55 °C, (2) = 40 °C, (3) = 25 °C, (4) = 10 °C



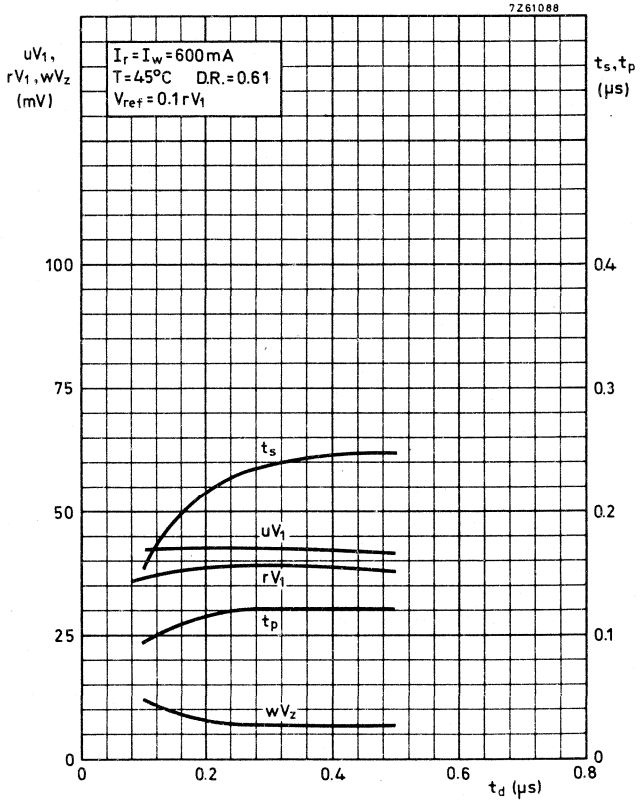
Typical core performance as a function of drive current at different temperatures and DR = 0.61.
(1) = 55 °C, (2) = 40 °C, (3) = 25 °C, (4) = 10 °C



Typical core performance as a function of current pulse rise time.



Typical core performance as a function of current pulse duration.

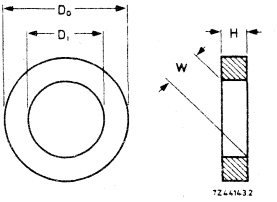


20 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA	
Switching time	0.200 µs
Medium temperature range	

DIMENSIONS

D_o = 0.540 mm (21 mil)
D_i = 0.340 mm (13.2 mil)
H = 0.140 mm (5.5 mil)
W = 0.141 mm (5.5 mil)



APPLICATION

This core has been developed for use in a coincident current memory, in particular in 3 D systems.

ELECTRICAL DATA

nominal operating conditions		
T_{amb}	25	°C
$I_r = I_w = I_{nom}$	800	mA
D.R.	0.50	
t_r (linear)	0.05	µs
t_d	0.24	µs

typical response values		
uV_1'	74	mV
rV_1	71	mV
wV_z	8	mV
t_p	0.110	µs
t_s	0.200	µs

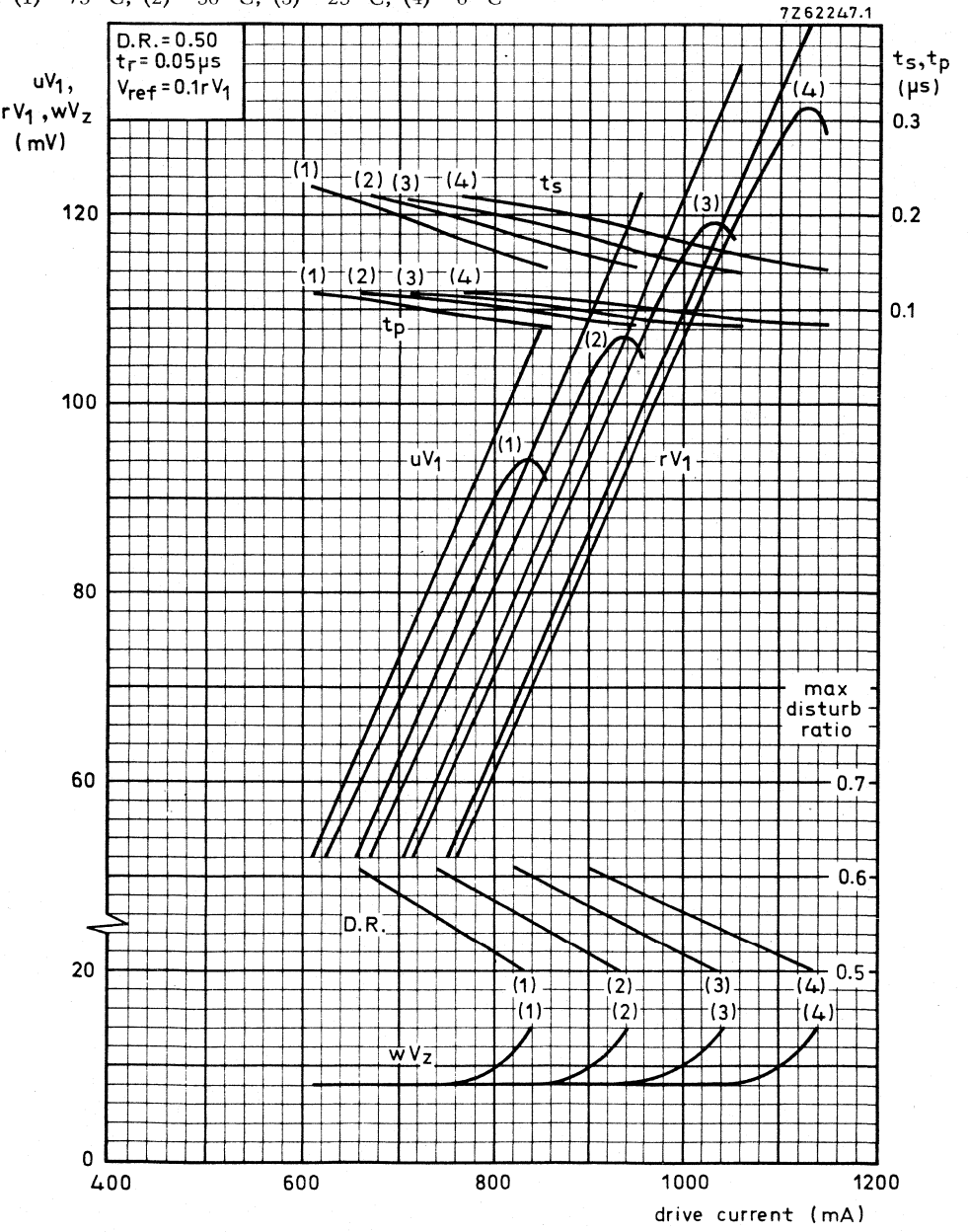
Drift with temperature (average over the range 0 to 75 °C)	
Rate of change of full drive current for constant uV_1	1.9 mA/°C
Rate of change of full drive current at break point and DR= 0.61	3.20 mA/°C
Rate of change of uV_1 for constant drive current	0.44 mV/°C

TESTS AND REQUIREMENTS

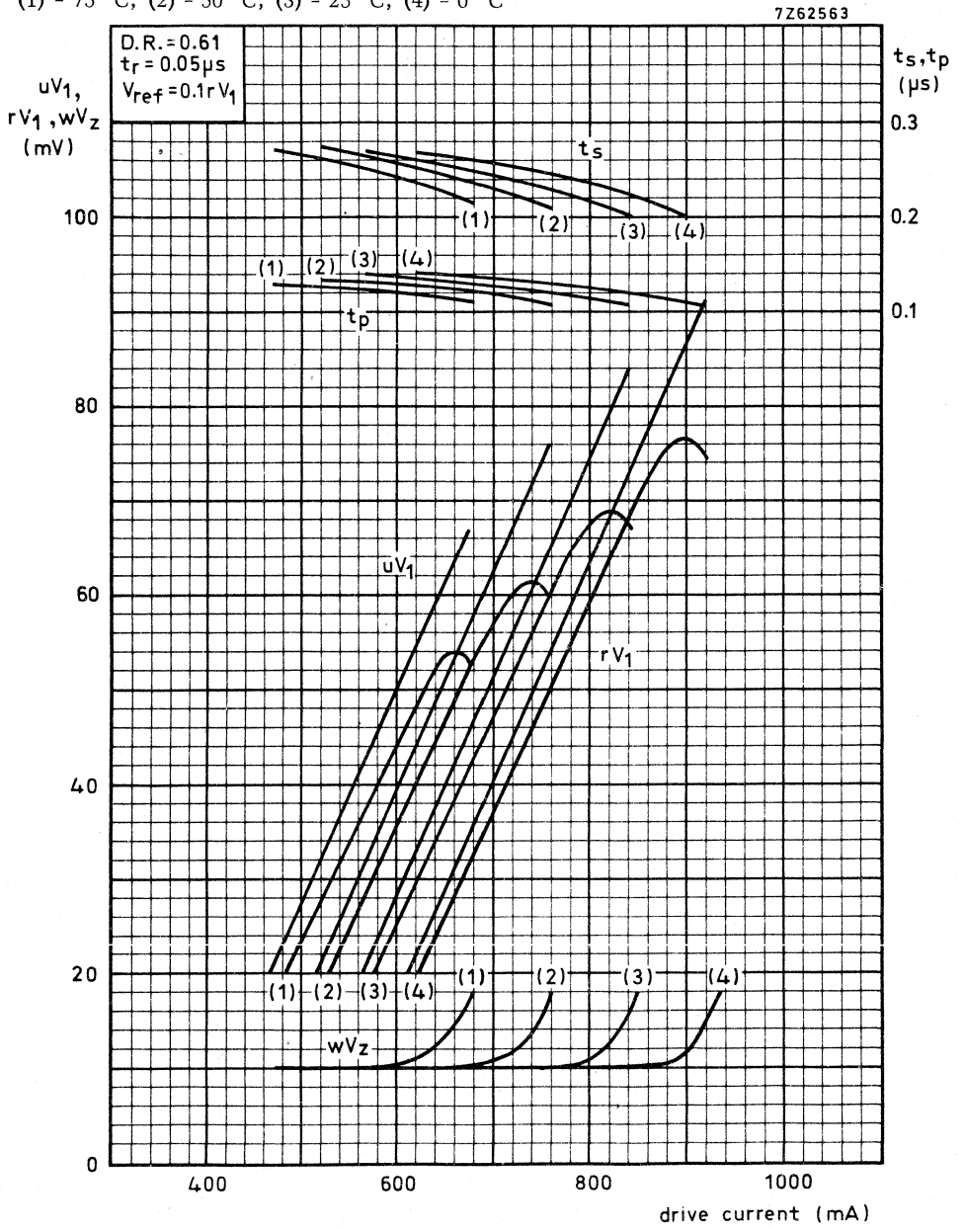
test conditions			equivalent at T_{amb} = 25 °C	
T_{amb}	75	°C		
$I_r = I_w$	620	mA	720	mA
$I_{pr} = I_{pw}$	378	mA	439	mA
D.R.	0.61		0.61	
Number of disturb pulses	32		32	
t_r (linear)	0.05	µs	0.05	µs
t_d	≥ 0.40	µs	≥ 0.40	µs
V_{ref}	5	mV	5	mV

acceptance limits and test conditions				
rV_1	50 ± 5	mV	53 ± 6	mV
wV_z	≤ 14	mV	≤ 13	mV
UR	≤ 8	mV	≤ 8	mV
t_p	0.120 ± 0.020	µs	0.120 ± 0.020	µs
t_s	0.230 ± 0.020	µs	0.230 ± 0.025	µs

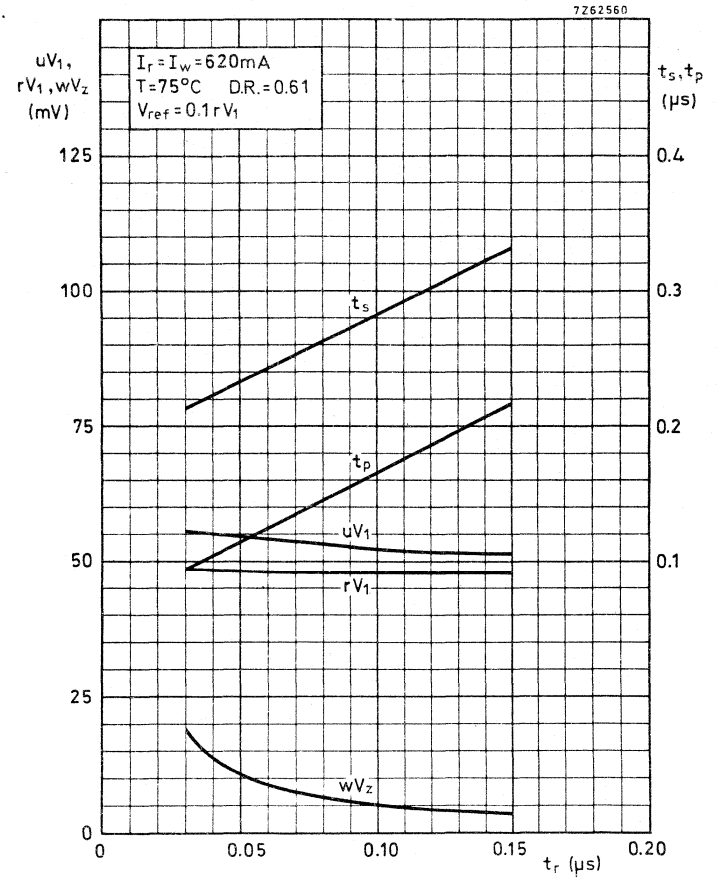
Typical core performance as a function of drive current at different temperatures and DR = 0.50
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



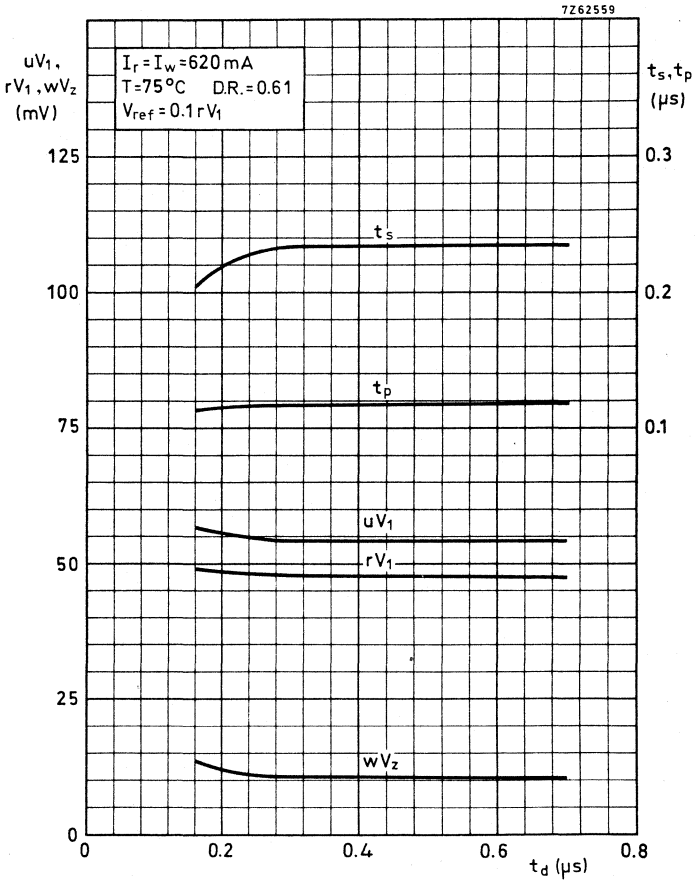
Typical core performance as a function of drive current at different temperatures and DR = 0.61
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



Typical core performance as a function of current pulse rise time.



Typical core performance as a function of current pulse duration.

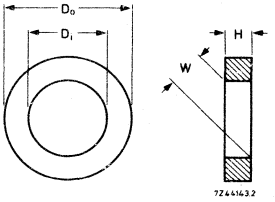


20 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA		
Switching time	0.21	μs
Medium temperature range		

DIMENSIONS

D_o = 0.540 mm (21.1 mil)
D_i = 0.340 mm (13.3 mil)
H = 0.127 mm (5.0 mil)
W = 0.150 mm (5.9 mil)



APPLICATION

This core has been developed for use in a coincident current memory, in particular in 3 D systems.

ELECTRICAL DATA

nominal operating conditions		
T_{amb}	25	°C
$I_r = I_w = I_{nom}$	800	mA
D.R.	0.50	
t_r (linear)	0.05	μs
t_d	0.25	μs

typical response values		
uV_1	64.0	mV
rV_1	61.0	mV
wV_z	8.5	mV
t_p	0.11	μs
t_s	0.21	μs

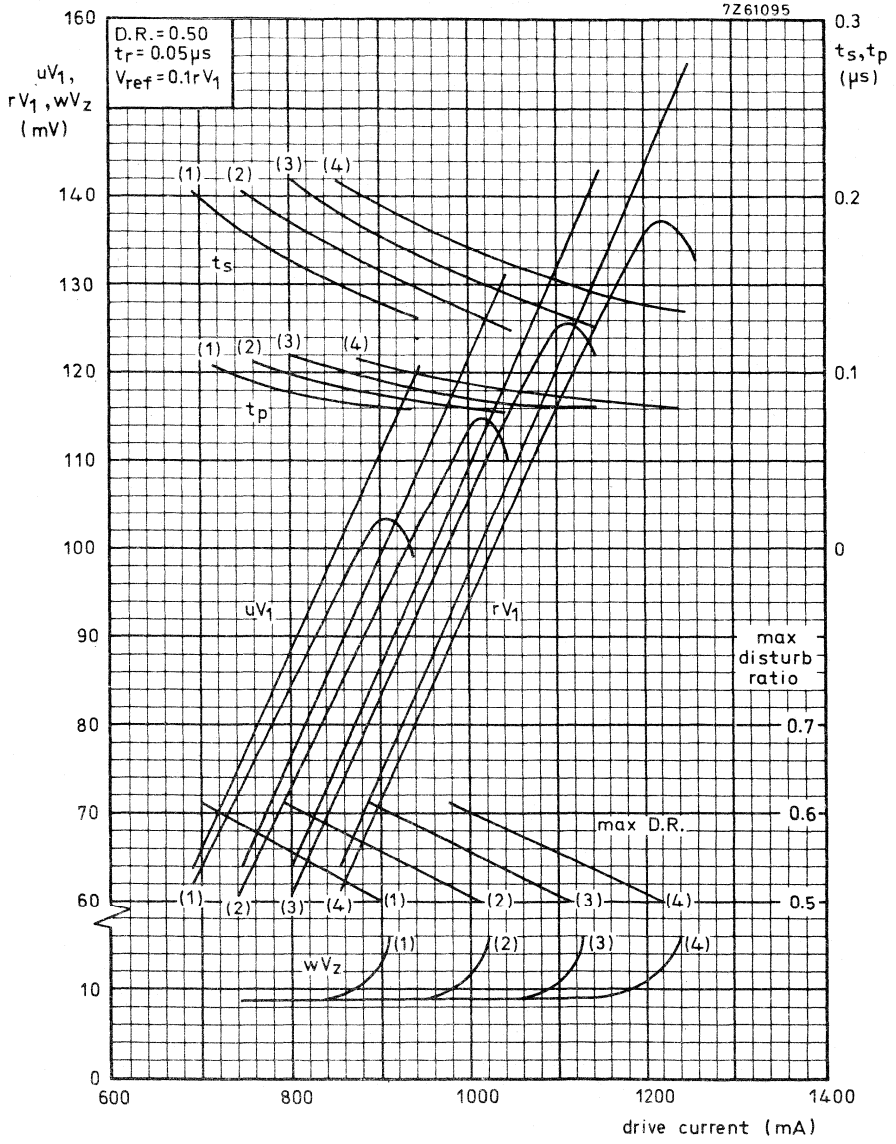
Drift with temperature (average over the range 0 to 75 °C)		
Rate of change of full drive current for constant uV_1	2.0	mA/°C
Rate of change of full drive current at break point and D.R. = 0.61	3.6	mA/°C
Rate of change of uV_1 for constant drive current	0.5	mV/°C

TESTS AND REQUIREMENTS

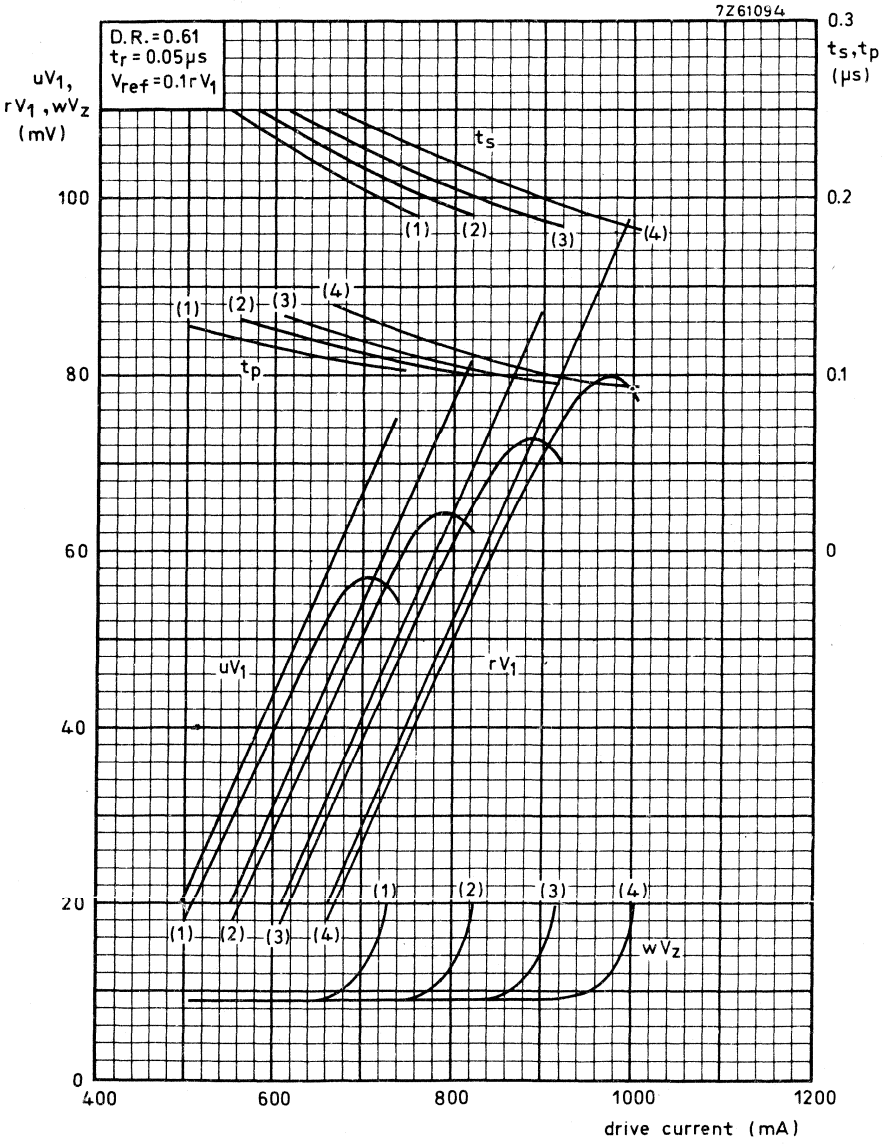
test conditions			
T_{amb}	75	25	°C
$I_r = I_w$	620	720	mA
$I_{pr} = I_{pw}$	378	439	mA
D.R.	0.61	0.61	
Number of disturb pulses	32	32	
t_r (linear)	0.05	0.05	µs
t_d	0.40	0.40	µs
V_{ref}	5	5	mV

acceptance limits at test conditions			
rV_1	44 ± 5	44 ± 6	mV
wV_z	≤ 12.0	≤ 12.0	mV
UR	≤ 6.0	≤ 5.5	mV
t_p	0.12 ± 0.02	0.12 ± 0.02	µs
t_s	0.23 ± 0.02	0.23 ± 0.025	µs

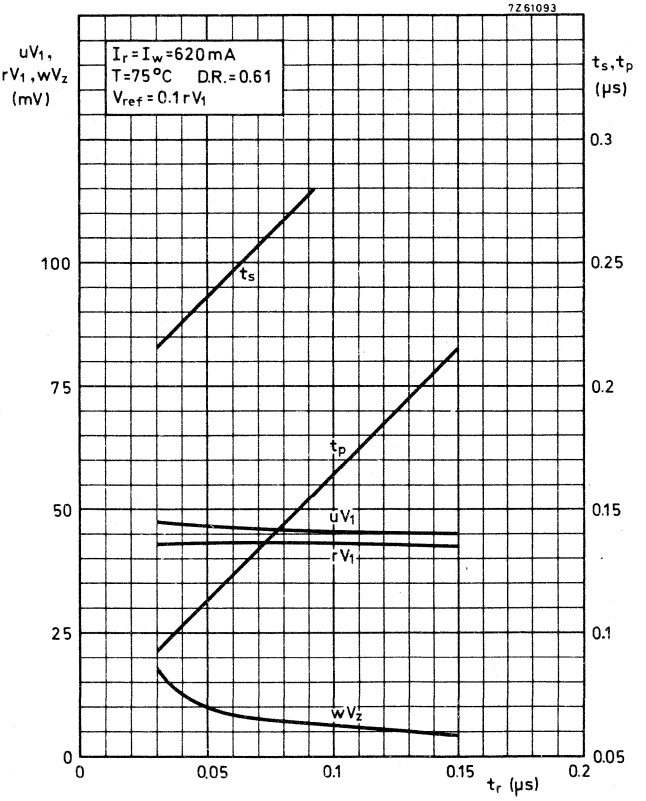
Typical core performance as a function of drive current at different temperatures and DR = 0.50
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



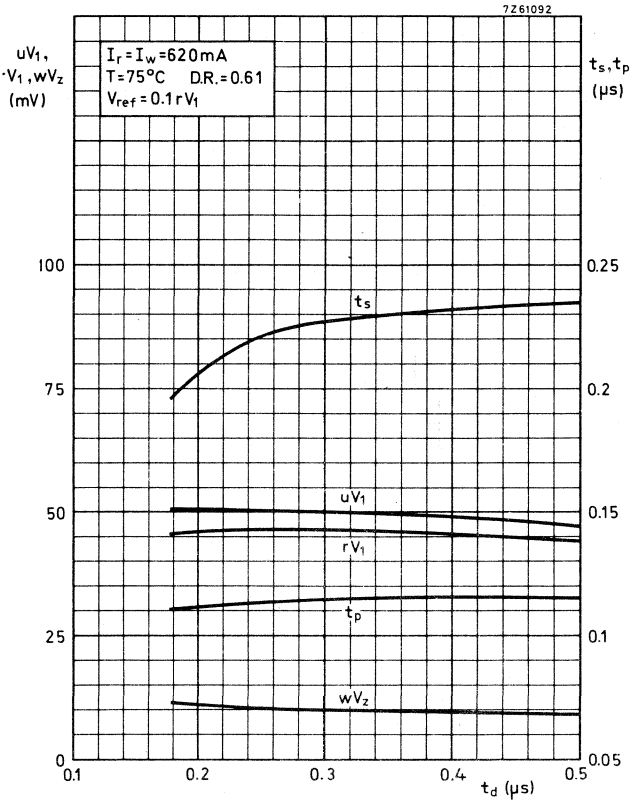
Typical core performance as a function of drive current at different temperatures and DR = 0.61
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



Typical core performance as a function of current pulse rise time.



Typical core performance as a function of current pulse duration.

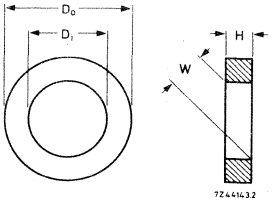


20 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA	
Switching time	0.210 μs
Medium temperature range	

DIMENSIONS

D_o = 0.540 mm (21.2 mil)
D_i = 0.335 mm (13.0 mil)
H = 0.100 mm (3.9 mil)
W = 0.166 mm (6.5 mil)



APPLICATION

This core has been developed for use in a coincident current memory, in particular in 3 D systems.

ELECTRICAL DATA

nominal operating conditions		
T_{amb}	25	°C
$I_r = I_w = I_{nom}$	973	mA
D.R.	0.50	
t_r (linear)	0.05	μs
t_d	0.26	μs

typical response values		
uV_1	52	mV
rV_1	51	mV
wV_z	4	mV
t_p	0.110	μs
t_s	0.210	μs

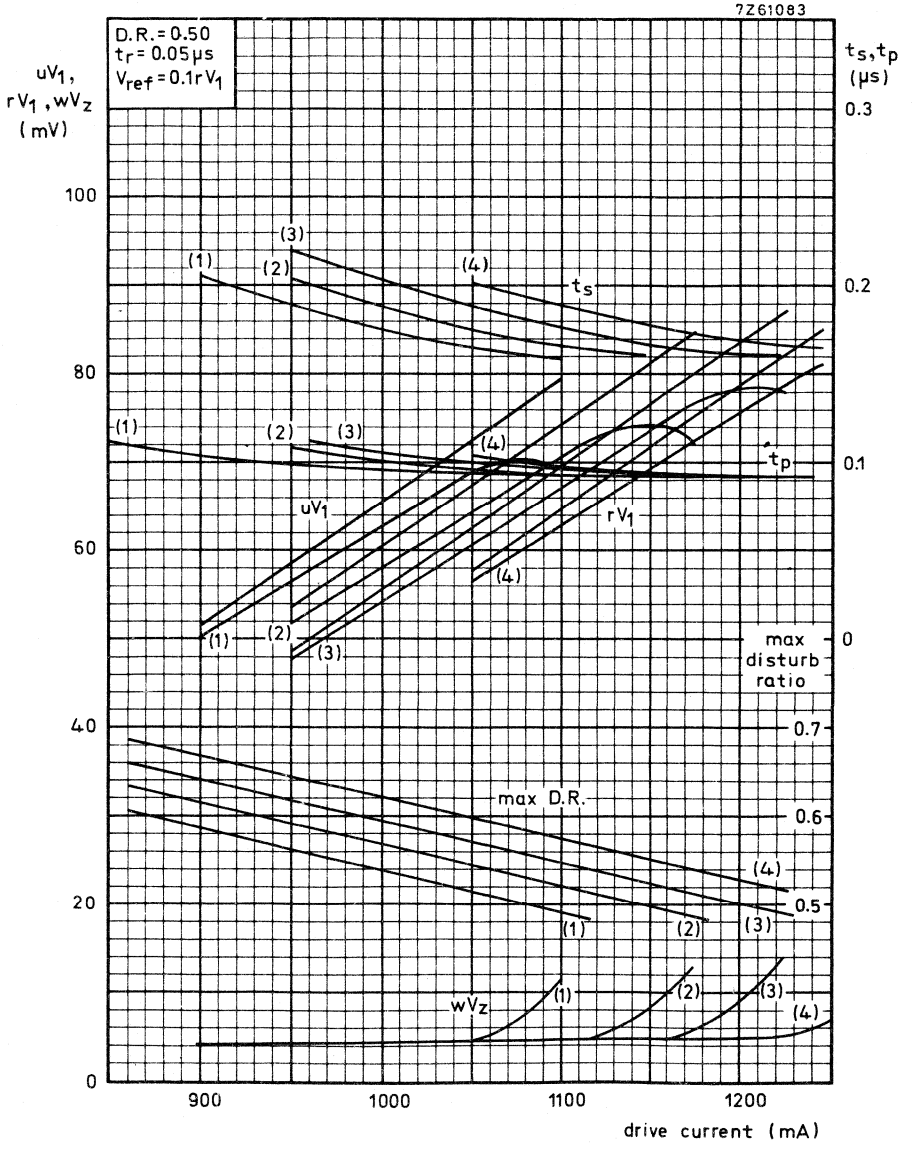
Drift with temperature (average over the range 0 to 75 °C)		
Rate of change of full drive current for constant uV_1	1.4	mA/°C
Rate of change of full drive current at break point and D.R. = 0.61	2.3	mA/°C
Rate of change of uV_1 for constant drive current	0.20	mV/°C

TESTS AND REQUIREMENTS

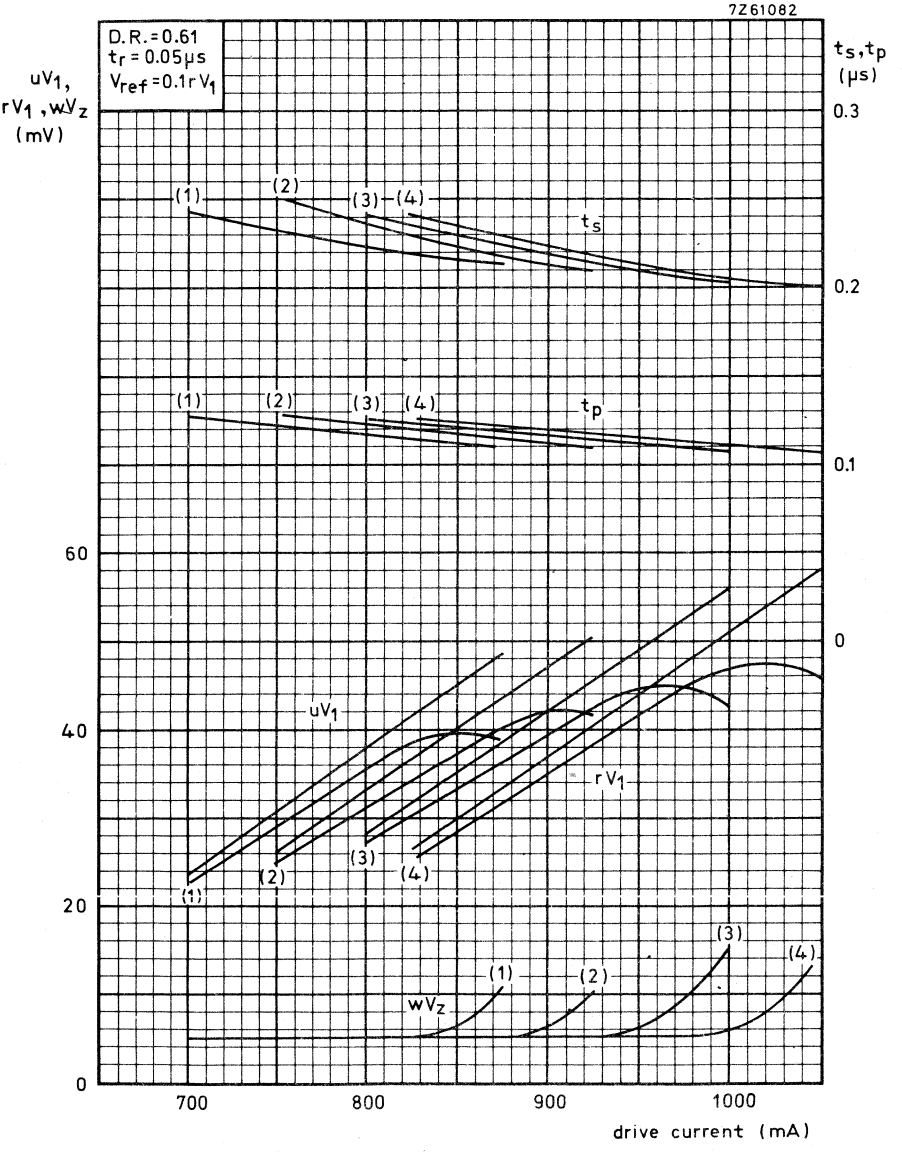
test conditions			equivalent at	
T_{amb}	70	°C	T_{amb} = 25	°C
$I_r = I_w$	810	mA	875	mA
$I_{pr} = I_{pw}$	495	mA	534	mA
D.R.	0.61		0.61	
Number of disturb pulses	32		32	
t_r (linear)	0.05	μs	0.05	μs
t_d	0.50	μs	0.50	μs
V_{ref}	5	mV	5	mV

acceptance limits at test conditions				
rV_1	36 ± 5	mV	37 ± 7	mV
wV_z	≤ 8	mV	≤ 8	mV
UR	≤ 5.5	mV	≤ 5.5	mV
t_p	0.105 - 0.145	μs	0.095 - 0.145	μs
t_s	0.195 - 0.235	μs	0.185 - 0.240	μs

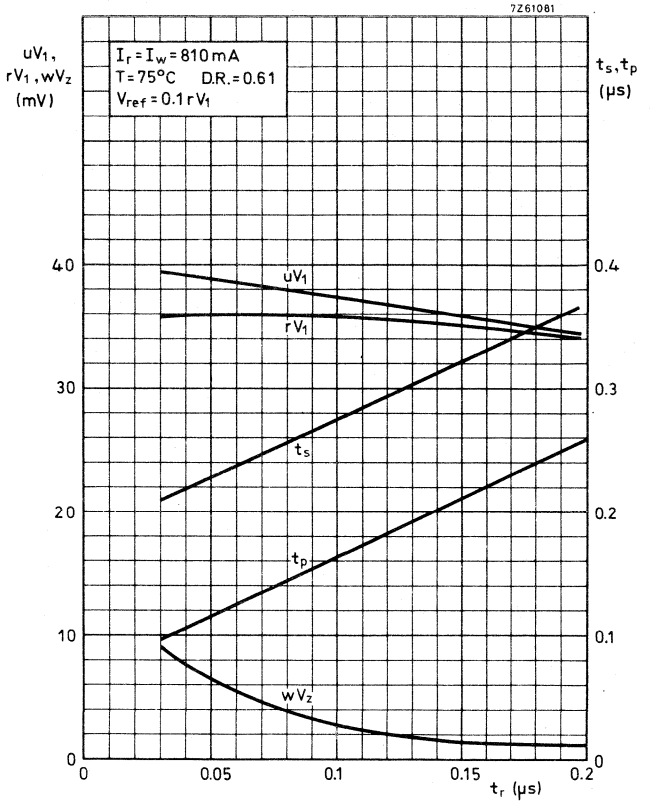
Typical core performance as a function of drive current at different temperatures and DR = 0.50
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C.



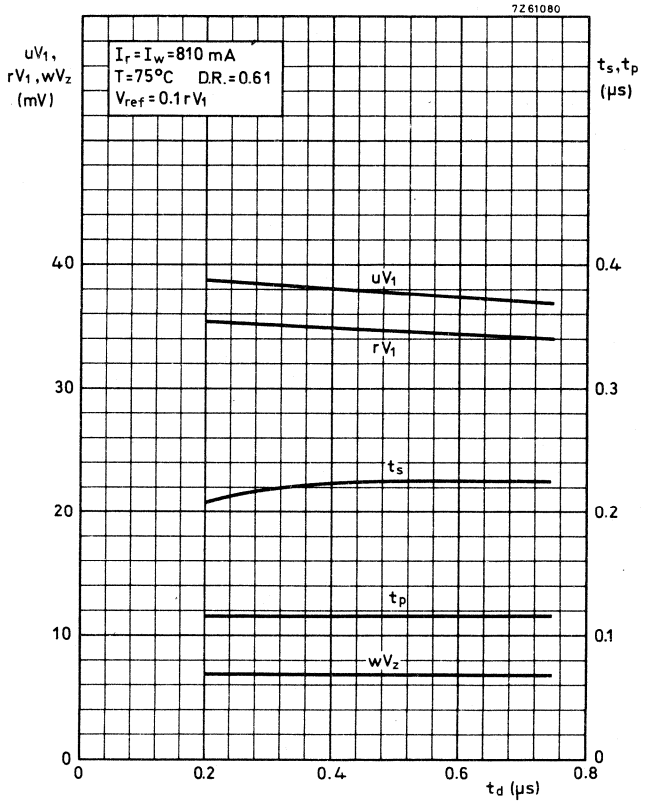
Typical core performance as a function of drive current at different temperatures and DR = 0.61
(1) = 75 °C, (2) = 50 °C, (3) = 25 °C, (4) = 0 °C



Typical core performance as a function of current pulse rise time.



Typical core performance as a function of current pulse duration.

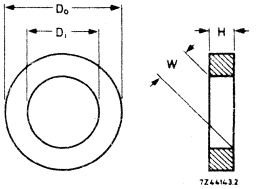


30 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA		
Switching time	0.40	μs
Standard temperature range		

DIMENSIONS

D_o = 0.813 ± 0.035 mm (32.0 mil)
D_i = 0.485 ± 0.035 mm (19.0 mil)
H = 0.165 ± 0.015 mm (6.4 mil)
W = 0.226 mm (8.8 mil)



APPLICATION

This core has been developed for use in coincident current memory, in particular in 3 D systems.

ELECTRICAL DATA

nominal operating conditions		
T_{amb}	25	°C
$I_r = I_w = I_{nom}$	710	mA
D.R.	0.50	
t_r (linear)	0.10	μs
t_d	0.50	μs

typical response values		
uV_1	63	mV
rV_1	61	mV
wV_z	5	mV
t_p	0.2	μs
t_s	0.4	μs

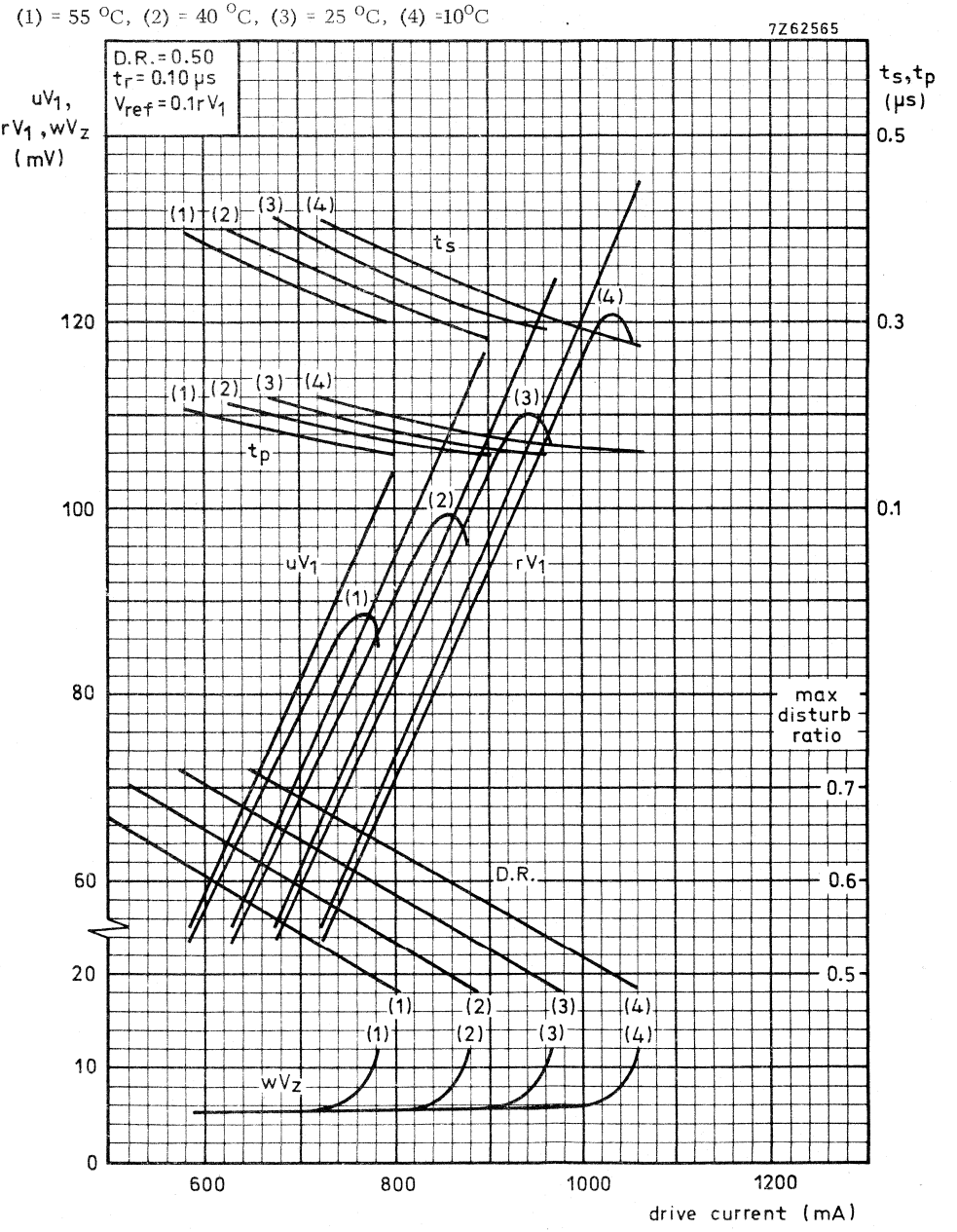
Drift with temperature (average over the range 10 to 55 °C)		
Rate of change of full drive current for constant uV_1	3.1	mA/°C
Rate of change of full drive current at breakpoint and DR = 0.61	5.1	mA/°C
Rate of change of uV_1 for constant drive current	0.7	mV/°C

TESTS AND REQUIREMENTS

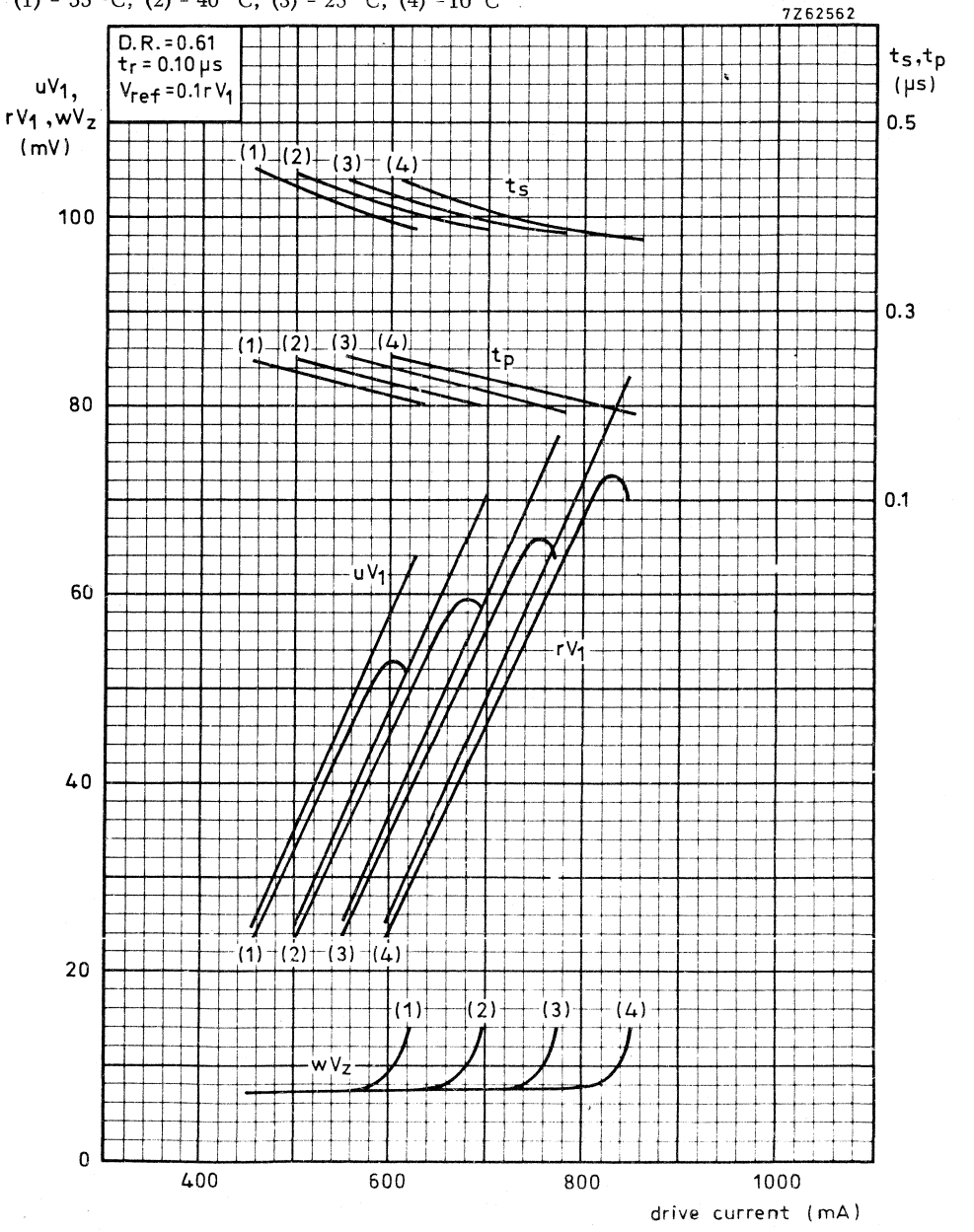
test conditions			equivalent at T_{amb} = 25	
T_{amb}	40	°C		
$I_r = I_w$	590	mA	640	mA
$I_{pr} = I_{pw}$	360	mA	390	mA
D.R.	0.61		0.61	
Number of disturb pulses	32		32	
t_r (linear)	0.10	µs	0.10	µs
t_d	1.50	µs	1.50	µs
V_{ref}	6	mV	6	mV
acceptance limits at test conditions				
rV_1	35-48	mV	35-48	mV
wV_z	≤ 9.5	mV	≤ 10.5	mV
UR	≤ 5	mV	≤ 5	mV
t_p	0.200-0.265	µs	0.200-0.265	µs
t_s	0.350-0.430	µs	0.350-0.430	µs

Typical core performance as a function of drive current at different temperatures and DR = 0.50

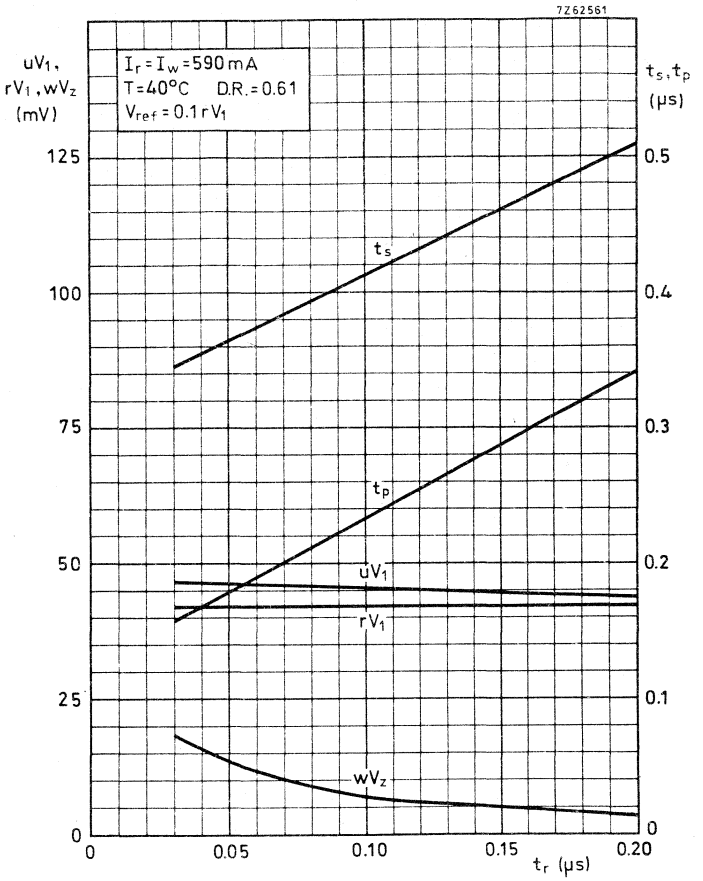
(1) = 55 °C, (2) = 40 °C, (3) = 25 °C, (4) = 10 °C



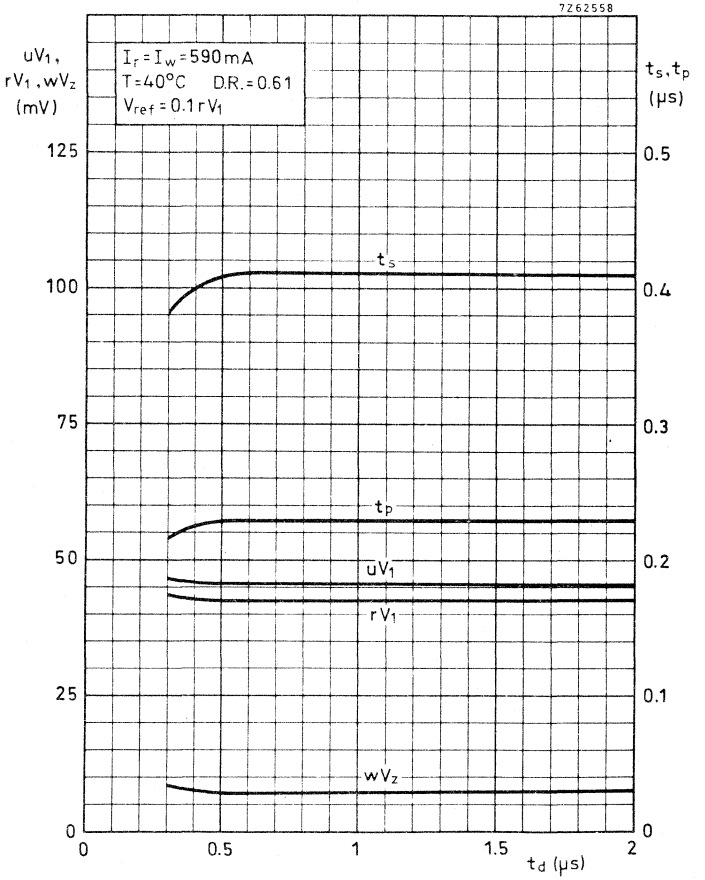
Typical core performance as a function of drive current at different temperatures and DR = 0.61
(1) = 55 °C, (2) = 40 °C, (3) = 25 °C, (4) = 10 °C



Typical core performance as a function of current pulse rise time.



Typical core performance as a function of current pulse duration.

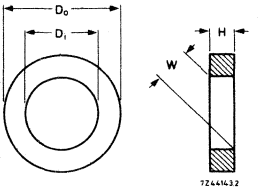


30 mil FERROXCUBE MEMORY CORE

QUICK REFERENCE DATA		
Switching time	0.49	μs
Medium temperature range		

DIMENSIONS

D_o = 0.82 mm (30 mil)
D_i = 0.49 mm (20 mil)
H = 0.21 mm (8 mil)
W = 0.20 mm (7.9 mil)



APPLICATION

This core has been developed for use in coincident current memory, in particular in 3 D systems.

ELECTRICAL DATA

nominal operating conditions		
T_{amb}	25	°C
$I_r = I_w = I_{nom}$	800	mA
DR	0.50	
t_r (linear)	0.15	μs
t_d	0.6	μs

typical response values		
T_{amb}	25	°C
uV_1	68	mV
rV_1	67	mV
wV_z	5	mV
t_p	0.27	μs
t_s	0.49	μs

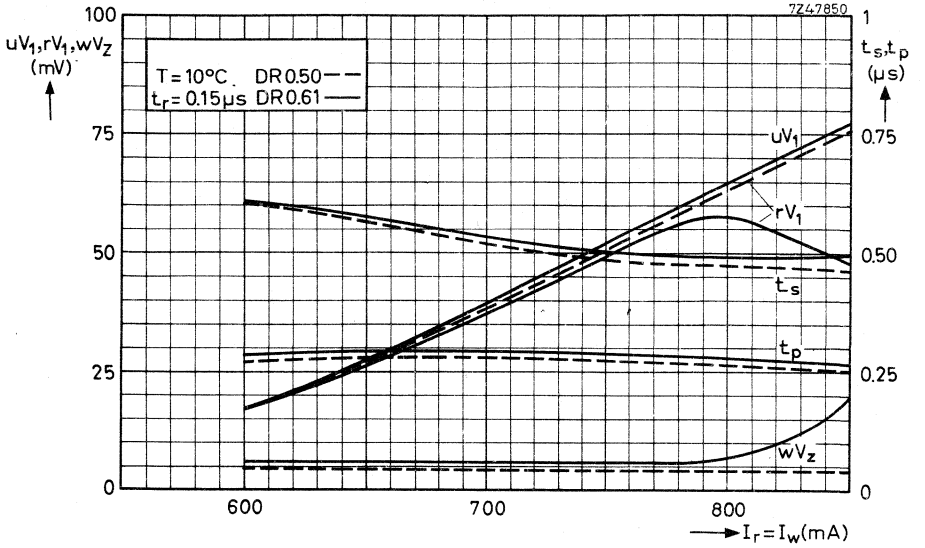
Drift with temperature (average over the range 0 to 75 °C)	
Rate of change of full drive current for constant uV_1	1.3 mA/°C
Rate of change of full drive current at break point and D.R.= 0.61	1.8 mA/°C
Rate of change of uV_1 for constant drive current	0.3 mV/°C

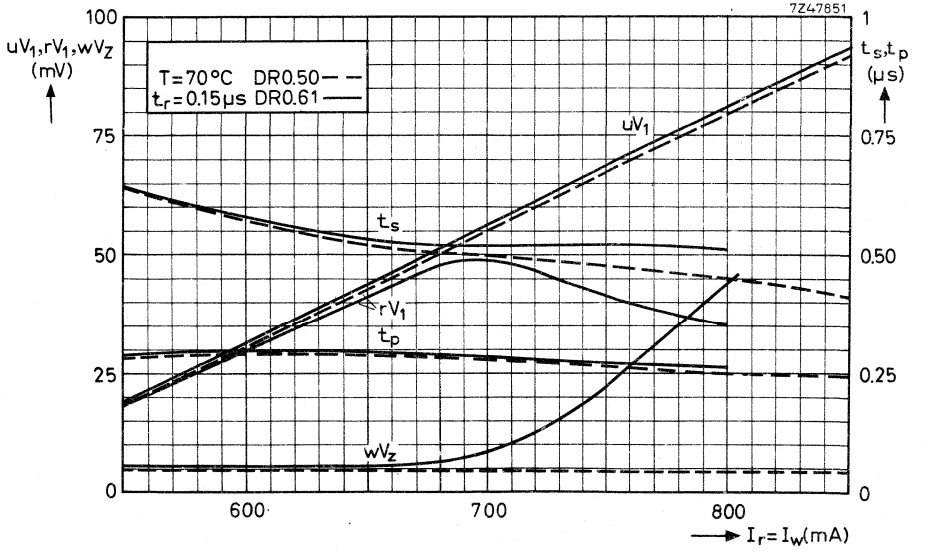
TESTS AND REQUIREMENTS

test conditions			
T_{amb}	10	70	°C
$I_r = I_w = I_{nom} - 10\%$	740	665	mA
$I_{pr} = I_{pw} = 0.5\, I_{nom} + 10\%$	450	405	mA
DR	0.61	0.61	
Number of disturb pulses	32	32	
t_r (linear)	0.15	0.15	µs
t_d	1.5	1.5	µs
V_{ref}	6	6	mV

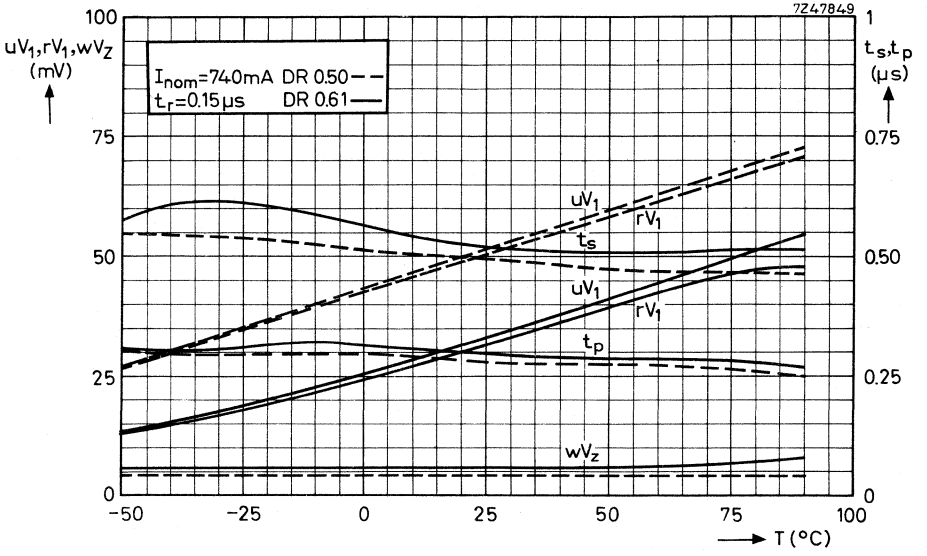
guaranteed values at specified test conditions			
rV_1	40 - 60		mV
wV_z	≤	8.5	mV
UR	≤	5.5	mV
t_p (10 °C)	0.265 - 0.345		µs
t_p (70 °C)	0.265 - 0.345		µs
t_s (10 °C)	0.440 - 0.545		µs
t_s (70 °C)	0.460 - 0.550		µs

Typical performance as a function of drive current at different temperatures.

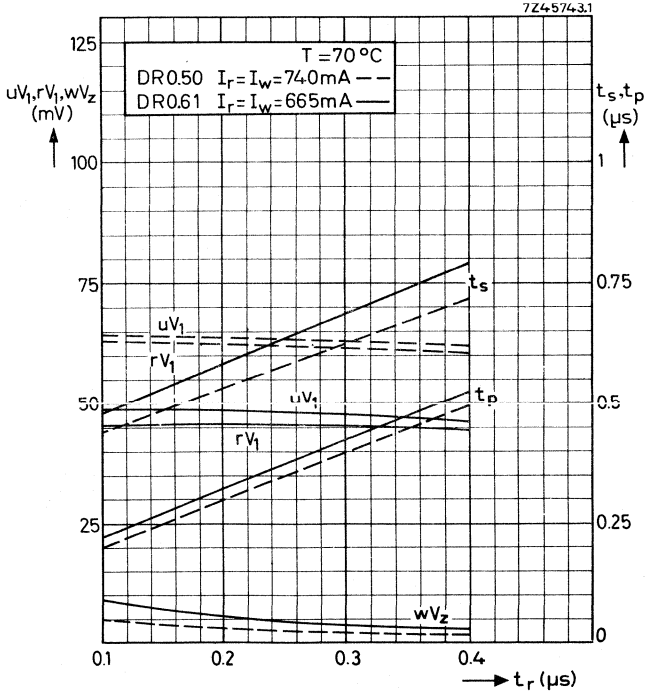




Typical performance as a function of temperature.



Typical performance as a function of current pulse rise time.



Matrix planes and stacks

INTRODUCTION

ORGANISATION OF FERRITE CORE MEMORIES

Memory cores work by virtue of their rectangular hysteresis loop. They have two major stable states and a threshold field. It is the latter property that makes it possible to arrange them in a matrix and access individual cores by a coincidence of row and column currents.

Since their introduction as memory elements, ferrite cores have steadily become smaller, faster and cheaper. Notwithstanding economies of batch fabrication promised by alternative magnetic and semiconductor devices, cores still predominate.

As cores themselves and the methods of manufacturing them have been subject to continuous development, so have the schemes for organising them into memories. For relatively small memories 3D organisation is generally best; when speed is important, a scheme of three wires instead of four can be adopted to make possible the use of smaller, faster cores. For mass memories 2D or $2\frac{1}{2}$D organisation is preferable, the former being more economic for long and the latter for short word lengths.

A survey of the different organisation systems is given below:

organisation	current pulses: read	current pulses: write	operation
2D	word current	word current + bit current	READ by a single current; WRITE by coincidence of 2 currents
3D	x current + y current; Z or inhibit current	y current + x current	READ by coincidence of 2 currents; WRITE by coincidence of 3 currents
2½D	x or bit current + y or word current	y or word current + x or bit current	READ by coincidence of 2 currents; WRITE by coincidence of 2 currents

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The characteristics of the different systems mentioned above are discussed in the following.

LINEAR SELECT 2D ORGANISED SYSTEM WITH 3 WIRES

In the past the matrices of word organised memories were supplied with two bit and one or two word lines through each core. As an example a 2D-array for 8 words of 4 bits with one word line is depicted in Fig. 1.

Writing (or restoration) of information in a core is performed by coincidence of two partial write current pulses with an amplitude I_{pw}, one contributed by the selected "word wire", the other by the selected bit wire. For writing a "0" the bit wire is not energized. In the given example the information 1011 is written in the memory. All the cores in the energized bit wires and disturbed by the partial write pulses I_{pw}. As the magnetic state of the half-selected cores must not be altered, the partial write current amplitude must not exceed a certain limit (break current).

The read (or clear) operation is effected by sending a full read current pulse (I_r) in opposite direction through the selected word wire, driving all the cores on this wire to the "0" state.

The output signals are sensed on the sense wire. There are no disturbed cores, so the read current amplitude is not limited by the core properties but only by the driving circuits. As a consequence of the higher read current which can be applied, faster cycle times are obtainable.

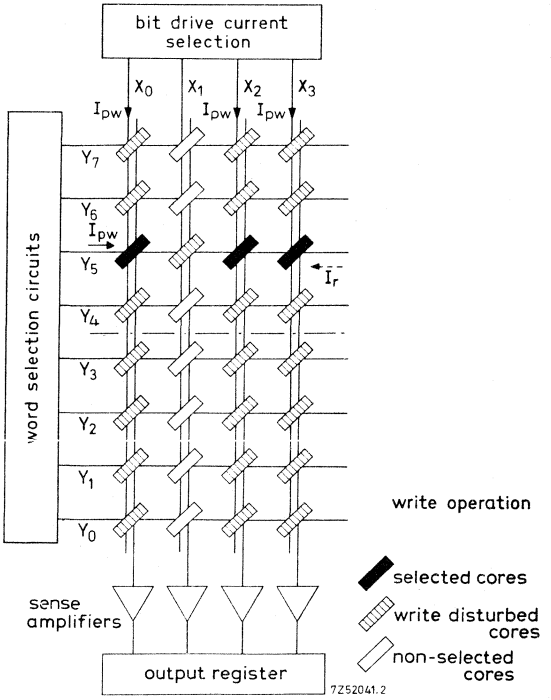

Fig. 1

LINEAR SELECT 2D ORGANISED SYSTEM WITH 2 WIRES

If, in a 2D system, the bit and the sense wire are combined, a two wire system is obtained. Threading two wires is obviously cheaper than threading three or four, especially for cores with a small diameter, and in very large memories, where the cost of the core array is significant. However, the most economical arrangement results in very long words, the number of bits per word being proportional to the square root of the total capacity in bits. Since all the bits are read simultaneously the bit transfer rate is high. The memory stack consists of two identical parts, each containing the complete number of bit lines and the half of the number of word lines. At one side each bit line is terminated with its characteristic impedance; the other side it is connected to the sense amplifier concerned. The bit/sense wire is split in two, to balance out the common mode noise generated by the bit current during writing, but at the expense of doubling the required bit current (see Fig. 2).

In fast memories the cycle time must be as short as possible. We have seen already that the read operation can be shortened by making $I_r > I_{nom}$. It is also possible to shorten the write operation by making $I_w > I_{nom}$. This can be achieved when applying a bipolar bit driver for the write operation. To write a "one" a current of $+\frac{1}{2} I_{nom}$ is sent through the bit wire and a current of $+I_{nom}$ through the word wire. A "zero" is obtained with the same word current, but with the bit current reversed ($-\frac{1}{2} I_{nom}$).
To read a word, a full current pulse $I_r \geq I_{nom}$ is sent through the selected word line so that a short access time is achieved.

Since each bit needs its own current driver, it is obvious that the driving circuits for 2D systems form an important part of the total cost. Despite of this disadvantage there is a growing interest in 2D systems for the following reasons:

- for mass memories with long word lengths, a high bit transfer rate can be achieved,
- less problems with discrimination of "one" and "zero",
- simple stack construction,
- the tendency towards steadily decreasing prices of the electronics.

Matrices based on the 2D/2 wire system are not standardized, but capacities of 4K144 and 4K288 are recommended.

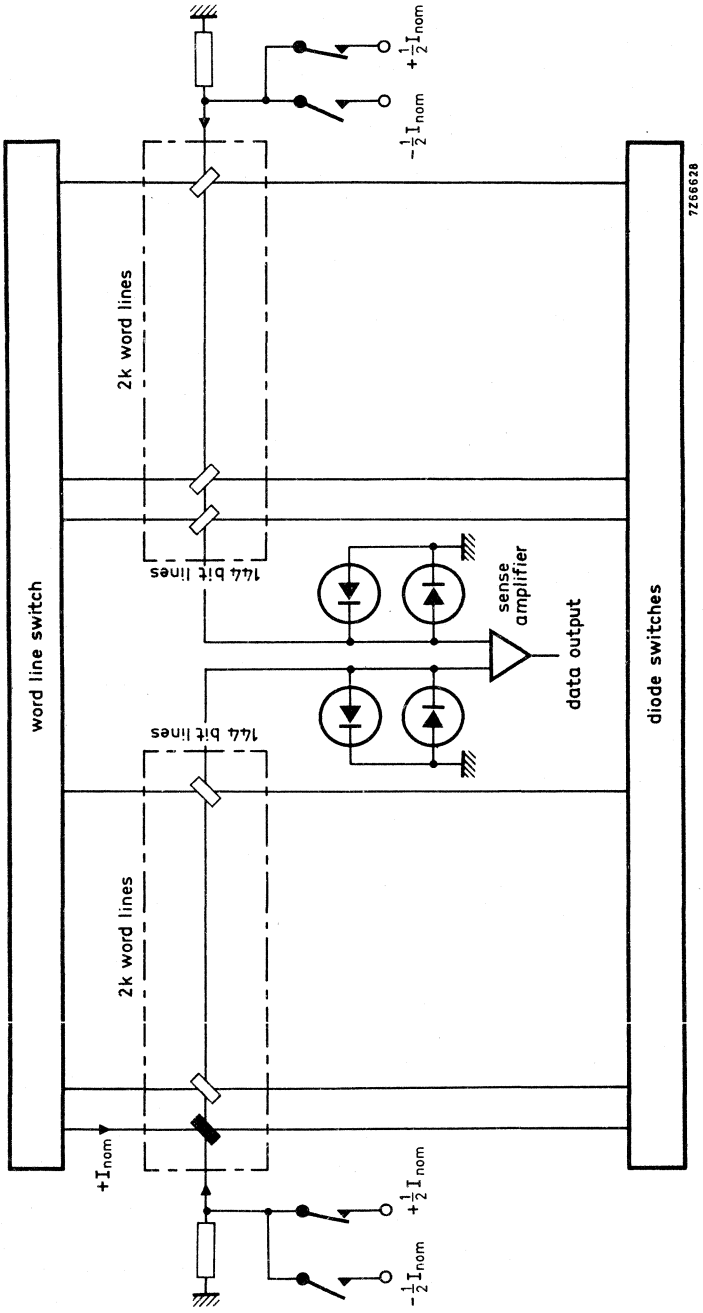

Fig. 2. Typical fast 2D/2 wire system in write operation for a 4k144 memory.

3D ORGANISED SYSTEM WITH 4 WIRES

The traditional 4-wire coincident current system provides a reliable and relatively inexpensive approach to the storage of information.
As an example a memory of 16 words, 4 bits is depicted in Fig. 3. The read or clear operation is effected by coincidence of two partial read pulses with an amplitude I_{pr}, one through the selected X line, the other through the selected Y line. The four fully selected cores are set to the "0" state, which induces a voltage pulse in each sense wire. The pulses are amplified and transferred to the output register as "ones" or "zeros" depending on the previous state of the cores.
The cores in the selected rows and columns are "read disturbed". The sense wires are threaded in such a way that the e.m.fs generated by the disturbed cores cancel each other.

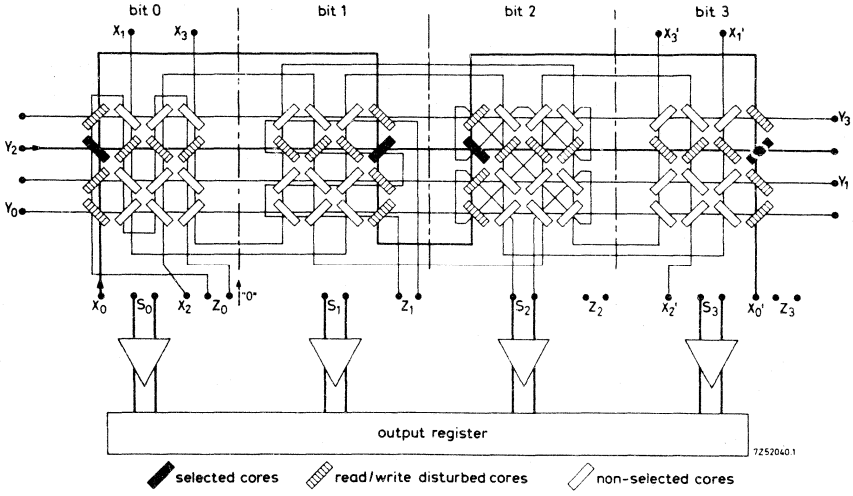

Fig. 3 3D array for 16 words of 4 bits.
In bits 0, 1 and 3 the S wire has been omitted, in bits 2 and 3 the Z wire.

After reading a word, new information can be written in the relevant cores by means of the corresponding X, Y and Z current drivers. For writing all "ones " partial write pulses (I_{pw}) are sent through the two selected X and Y wires, as for the read operation, but in opposite direction. In Fig. 3 the cores X_0Y_2 (solid) have been selected for storing the word 1111, while the other cores (hatched) in the selected rows and columns are "write disturbed".
For writing a "zero" the same X and Y pulses are needed as for writing "ones", but switching to the "one" state must be prevented by sending an opposite partial write pulse ($-I_{pw}$) through the Z wire concerned. (The Z wire may run parallel to the X wires in one matrix and parallel to the Y wires in another, see bits 0 and 1 in Fig. 3). All cores situated on a non-selected row or column are read disturbed, generating inhibit noise on the sense wire. The inhibit noise should be damped out before a successive read operation

may start.
As cores are disturbed during the read and the write operations, the read, write and inhibit currents must have an upper limit.

If it is impossible to arrange all cores of a large memory in one plane, the cores will be distributed over a number of stacked matrix planes. This also has the advantage that the number of bits can be easily extended. A simple stack set-up is depicted in Fig. 4.
Since the number of selection circuits is minimal if the core array is a square with sides of 2^n cores, our matrix planes are standardized on the sizes 32 x 32, 64 x 64, and 128 x 128 bits.

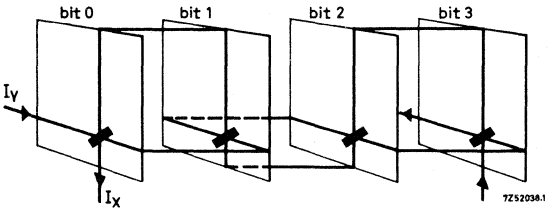

Fig. 4. Principle of series connection of the X wire and of the Y wire for one word of four bits in the 3D system.

Advantages of the 3D system are:

1. Inexpensive selection system.
2. Memories up to 10^6 bits can be realized.

Disadvantages are:

1. Limited temperature range in fast memories due to inhibit dissipation.
2. Upper limits for all drive currents.

3D ORGANISED SYSTEM WITH 3 WIRES

Using the same wire for inhibit and sense leads to a 3D/3 wire system; the resulting simplification of wiring is of great advantage, especially for the wiring of small cores. The inhibit/sense wire is split into two equal parts. For the inhibit driver these parts are connected in parallel and driven simultaneously; for the sense amplifier they are series-connected. For this reason the cores must be arranged e.g. in a double herring bone pattern, and the inhibit driver must supply the full drive current (see Fig. 5).

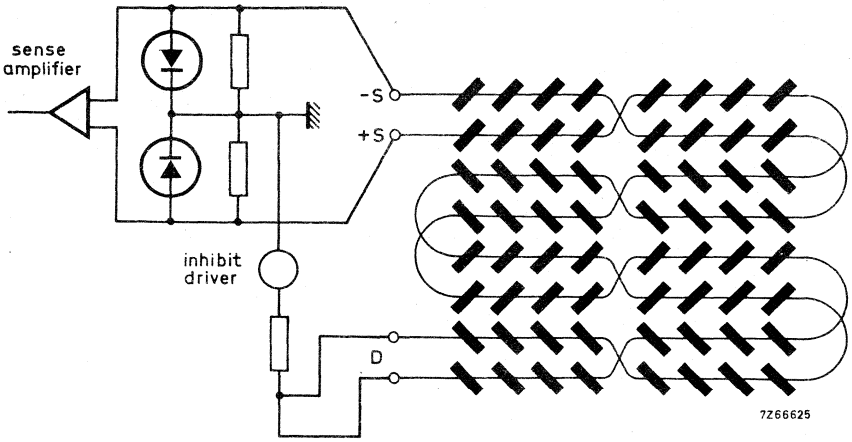

Fig. 5 Sense/inhibit line configuration.
S = sense, D = inhibit.

The 3D/3 wire matrix stack is in most cases a planar construction, i.e. all bits and relevant diodes are on one printed wiring board.
An additional advantage of this construction is that the drive wires can be continuous (see Fig. 6), resulting in a considerable reduction of the number of solder joints.
Fig. 6 shows that all cores in a horizontal row are parallel to each other positioned. This makes it possible to decrease the pitch to less than the core diameter, resulting in a considerable reduction of sense/inhibit wire length.
By mounting the selection diodes close to the core arrays, stray inductances are minimized permitting faster cycle times.

By comparison with the conventional stacked plane construction the 3D/3 wire system offers the following important advantages:

- higher reliability due to fewer soldered joints
- small size, resulting in : lower inhibit dissipation
  lower sense wire attenuation
  faster cycle times

The 3D/3 wire planar construction meets today's requirements, especially in mini computer applications.

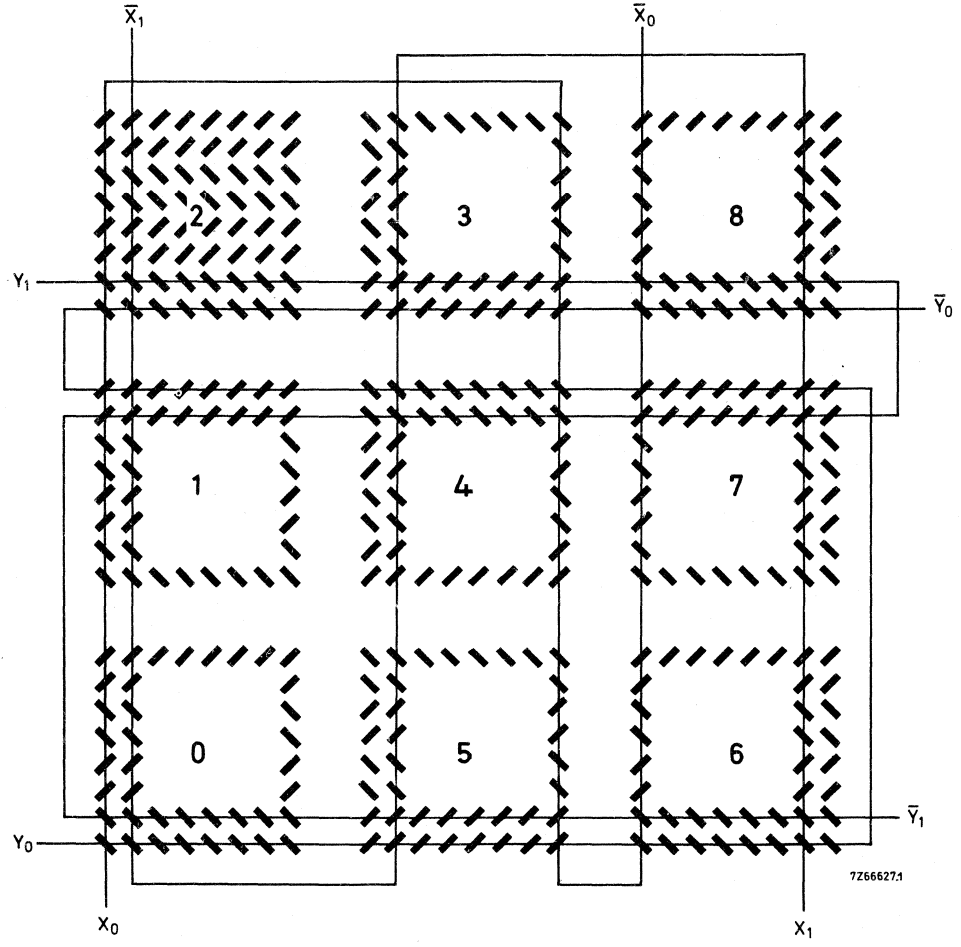

Fig. 6 Typical drive wire diagram for a 64 words/9 bits plane

2½D ORGANISED SYSTEM WITH 3 WIRES

This is a three-wire hybrid of the 2D and the 3D system. An X, a Y and an S wire are threaded through each core. Reading of information conforms to the 3D system and writing conforms to the 2D system. Thus, for reading and for writing "ones" two coincident partial drive currents are needed (I_{pr} and I_{pw}, respectively); for writing "zeros" the X wires are not energized.

The sense wire can be laid along the X wires, see Fig. 7, or threaded diagonally as in the 3D system. The twist in the middle of the S wire is for mutual cancellation of disturb signals generated in the upper and lower part of the columns.

To obtain equal propagation delay times for the X and Y drive lines, the total number of columns (length of the Y wire) should be about equal to the number of rows (length of the X wire), which is why the matrices for each bit have an oblong form.

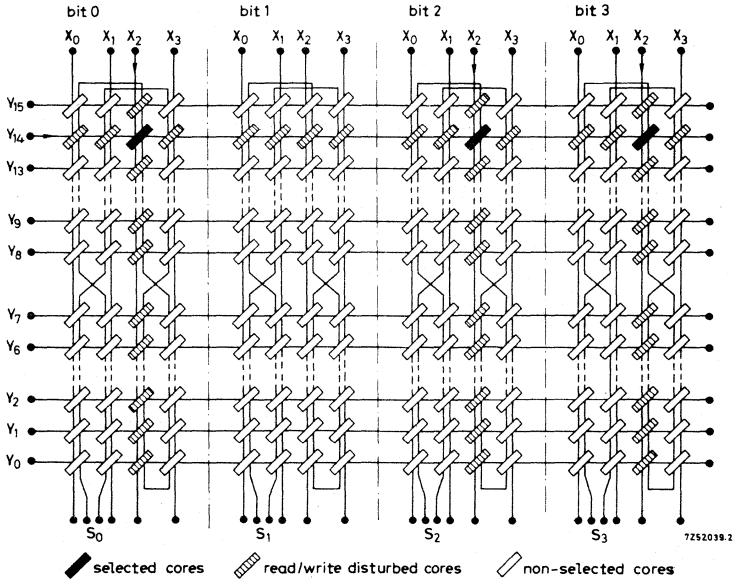

Fig. 7. $2\frac{1}{2}$D matrix plane for 64 words of 4 bits. The arrows indicate the writing of the word 1011.

In the read operation each sense wire receives much more noise from the disturbed cores of the selected column than from the cores of the selected row. This noise can be reduced to improve the discrimination between "ones" and "zeros" by reading in the staggered mode.

In the staggered read mode the I_{prx} pulse starts some nanoseconds earlier than the I_{pry} pulse. The selected core is read during the latter so that only the disturb signals from the selected short row contribute to the noise level. The resulting good discrimination between "1" and "0" signals permits a larger number of cores per sense line (words per bit). The time lost due to the staggered read mode is amply compensated by the time gained due to the absence of a recovery time for inhibit noise.

The $2\frac{1}{2}$D system has the following advantages:

1. Minimal heat dissipation in the matrix.
2. No inhibit noise on the sense wire.
3. Faster cycle times can be obtained.
4. The bit diodes can be easily mounted on the printed-wiring board.

Since each bit needs its own selection circuit, the $2\frac{1}{2}$D system finds its application primarily in memories with a large number of words and a small number of bits. The most economical number of bits is 18.
Matrix planes based on the $2\frac{1}{2}$D system are not standardized, but capacities of 16K18 and 32K18 are recommended.
A complete $2\frac{1}{2}$D stack will be delivered with the interconnections for the bit and word lines, and includes the bit as well as the word diodes.

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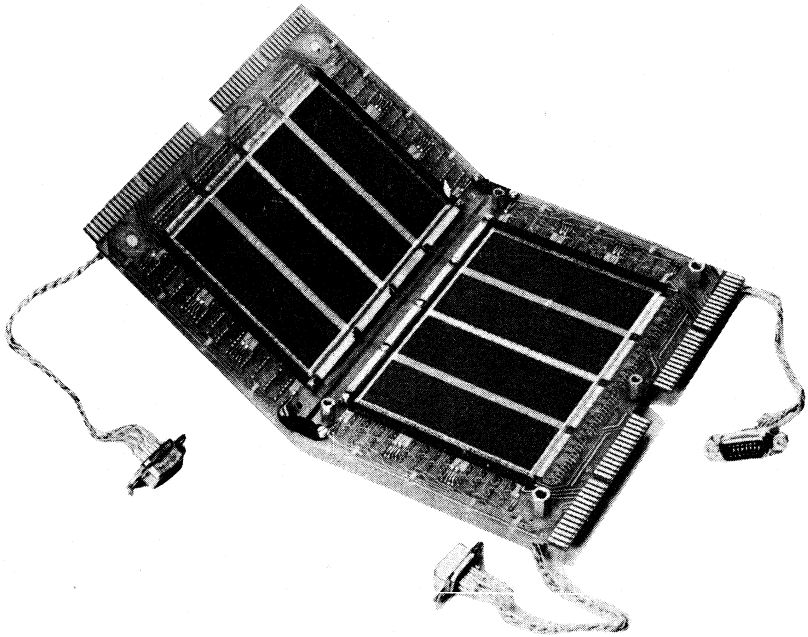


A pluggable $2\frac{1}{2}$D 16k6 stack with bit diodes.

2½D ORGANISED SYSTEM WITH 2 WIRES

By combining the sense and bit wires, it is possible to achieve $2\frac{1}{2}$D operation with only two wires through each core. Although this will introduce problems in electronics and cause some loss of performance, the advantage of having to thread only two wires may be worthwhile in mass memories in which cost per bit is more important than speed. Fig. 8 shows a simplified diagram for one bit in a $2\frac{1}{2}$D/2 wire set-up. The Y or bit current is switched to two wires in parallel, for writing as well as for reading, to balance out the disturbing voltages across the secondary winding of the transformer. The word lines are operated in staggered mode. The two bit wires selected for reading also function as sense wires for the selected core. From the selected pair of cores in the figure the left one will be energized in coincidence, the right one in anticoincidence. With the word current reversed the left core will be energized in anticoincidence and the right one in coincidence.

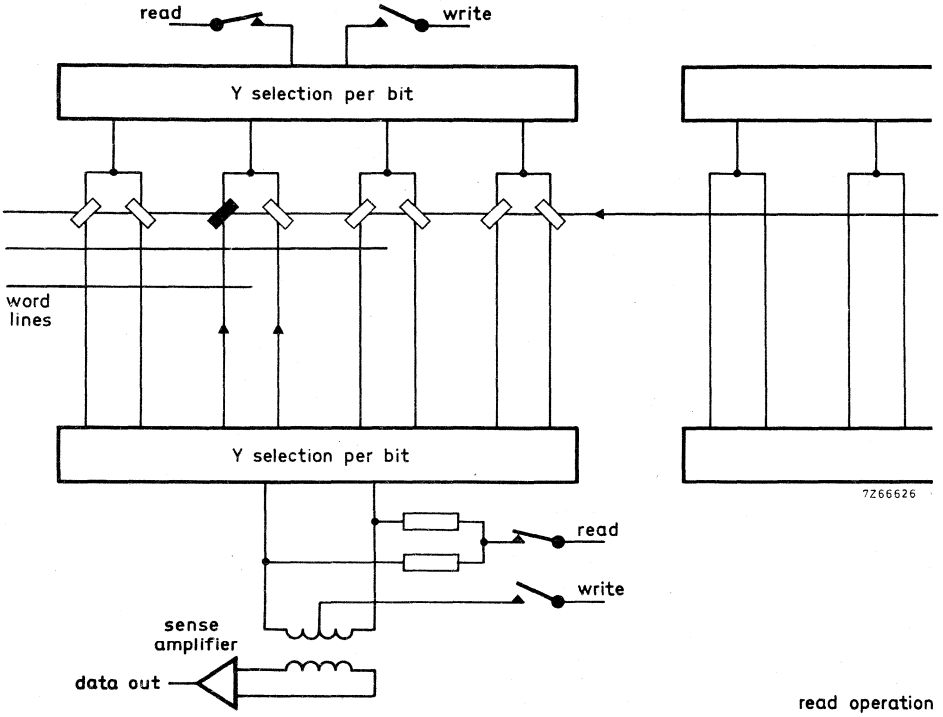


Fig. 8

This system must be perfectly balanced to prevent an output voltage on the secondary winding of the transformer. But in practice there will always be some unbalance due to differences of d.c. resistances of the Y drive lines, differences in the selection switches and diodes, and the delta noise of the half-selected cores on the Y drive lines. These factors may introduce noise amounting to several volts when the bit current is switched on. Therefore, the noise must be given time to die out before the word current can be switched on, so the imperfections of the whole system will directly influence the speed. For $2\frac{1}{2}D/2$ wire systems a good compromise must be found between cost and speed.

TEST METHOD

All cores in each plane are tested to make sure that they satisfy the core specification. Planes are tested at 23 ^{o}C with marginal drive currents.
Each core is tested with the pulse patterns shown on next page.

The "1" output of each core is measured with all cores in the "1" state (best pattern). The cores are tested to guarantee a minimum "1" output at max. and min. values of switching and peaking time (t_s and t_p).

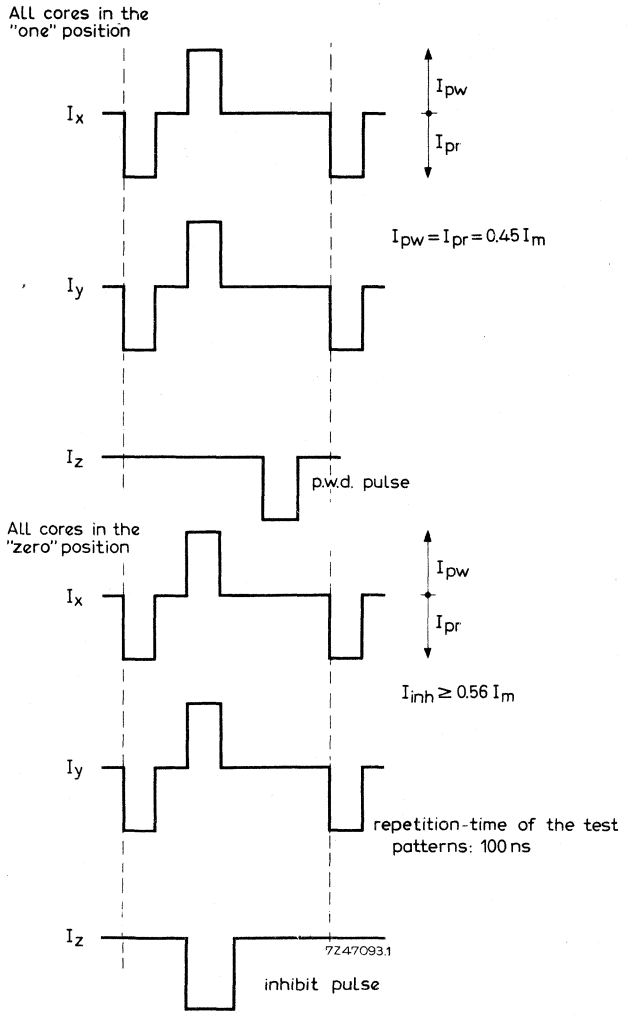
Furthermore, the disturb sensitivity of the cores is tested by increasing the disturb ratio up to at least 0,62.
This is done by measuring the output with and without a post-write disturb (p.w.d.) pulse. If the difference of these values exceeds a given limit, the core is replaced. This is also a check on whether the sense wire passes through all cores.

The "0" output of each core is measured with all cores in the "0" state (best pattern). The cores are tested to guarantee maximum permissible "0" output. This also checks whether the inhibit wires pass through all cores and whether the noise cancellation of the sense wire is adequate.

Sample tests are carried out with all the cores set in worst pattern, checking the peak value of the "0" output (peak delta noise) and the "0" output at peaking time of the "1" output.

Besides the electromagnetic testing, the planes are tested for insulation resistance and for the d.c. resistance of the wiring.

After complete assembly (including selection diodes, where applicable) a stack is functionally tested.


All cores in the "one" position
I_x
I_{pw}
I_{pr}
$I_{pw} = I_{pr} = 0.45\, I_m$
I_y
I_z
p.w.d. pulse
All cores in the "zero" position
I_x
I_{pw}
I_{pr}
$I_{inh} \geq 0.56\, I_m$
I_y
repetition-time of the test patterns: 100 ns
I_z
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inhibit pulse

ORDERING INFORMATION

Three ordering procedures can be distinguished:

1. Repeat orders. Your original order will have been allocated a 12-digit catalogue number. Please use this number.
2. Orders for products from this handbook. Relevant 12-digit catalogue number must be mentioned.
3. Orders for products adapted to customer requirements. These must be accompanied by a specification.

For new memory stacks it is important to make use of the standard matrices mentioned in this book to save cost and delivery time.
To avoid misunderstandings the additional requirements must be mentioned correctly. Therefore, a specification checklist has been printed below, which we ask you to complete as far as possible.

CUSTOMER SPECIFICATION CHECKLIST

Customer		d.d.
ELECTRICAL REQUIREMENTS		
Stack capacity	words,	bits
Organisation	3D/4 wire 3D/3 wire	$2\frac{1}{2}$D/3 wire $2\frac{1}{2}$D/2 wire
		2D/3 wire 2D/2 wire
Catalogue number		
Required cycle time	µs	
Core type		
With/without selection diodes		
With/without lead-off wires		
MECHANICAL REQUIREMENTS		
Maximum overall dimensions available		
length	mm	
width	mm	
height	mm	
Required length of free threaded end of fixing screws:		mm
ENVIRONMENTAL REQUIREMENTS		
Ambient temperature range	°C	
Storage temperature range	°C	
Relative humidity	%	
Shock	g	
Vibration, frequency range acceleration	Hz g	
SPECIAL REQUIREMENTS		

3D/3-WIRE PLANAR MEMORY STACKS

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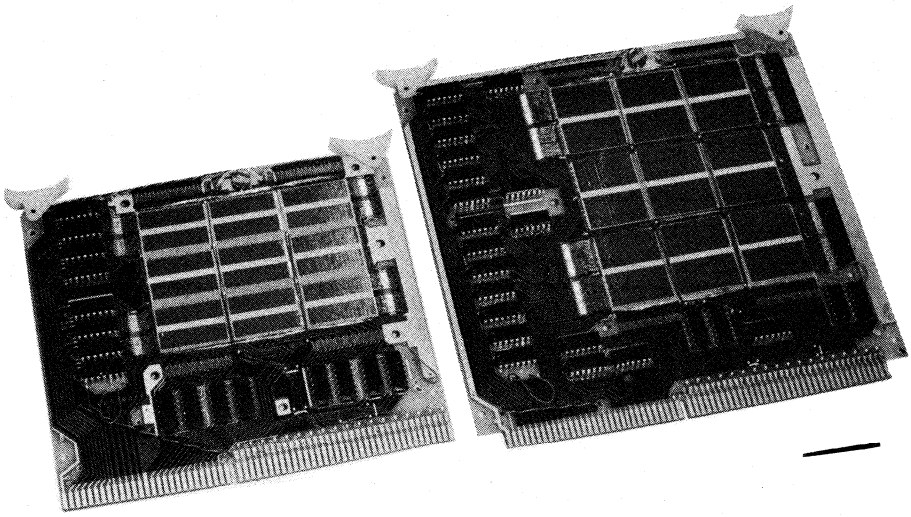


4k18 stack

8k18 stack

INTRODUCTION

Faster cycle times and lower cost have caused a growing interest in memory stacks with planar construction, and especially for the 3D/3 wire system. Compared with the conventional stacked-plane construction the planar system has the following advantages:

1. Continuous wiring of the drive wires is employed which considerably reduces the total number of soldered joints. Not only does this improve circuit reliability but the design of the printed circuit board is simplified and made more reliable.
2. Cores can be laid out in parallel on pitches smaller than the core diameter. A smaller core-area results which, in turn, means smaller drive current delay times allowing faster cycle times to be achieved. There is a lower inhibit dissipation, and also lower sense-wire impedances giving a reduction in response attenuation.
3. Selection diodes and switches can be placed very close to the core area thereby reducing inductances and again improving cycle times.
4. As all the bits are laid out in one flat area, heat dissipation is good over the whole plane and temperature differences between the bits are small.

PLANAR STACKS WITH 18 mil CORES

Description

In offering planar stack construction we offer the most modern type of stacks. The planar stack consists of 2 identical matrices of 9 wired core arrays. The double herringbone core arrays are continuously wired on both sides of the printed circuit board. Drive wires are interconnected from one side of the printed circuit board to the other through metallized-through holes (see Fig. 1a).

Doubling the word capacity is achieved by turning the core arrays of one matrix through 180° as shown in Fig. 1b. Half of the cores are now driven in coincidence and half in anti-coincidence, therefore information is written into the anti-coincidence cores by reversing the Y drive current. This operation is called current phasing.

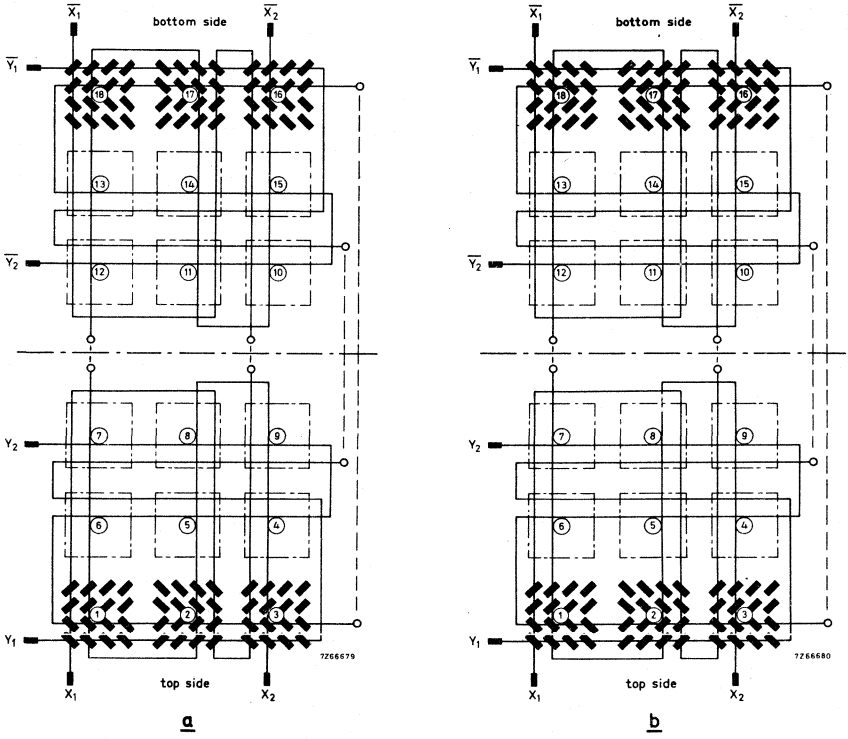
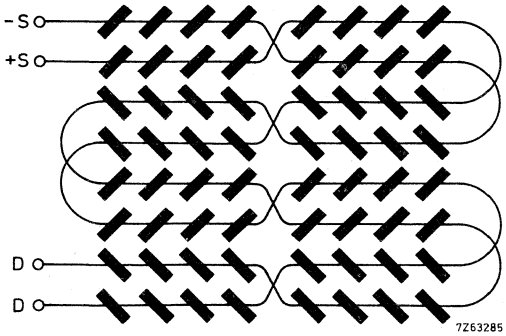


Fig. 1 Core arrays and X and Y line wiring scheme.
a. For 4k18 memory
b. For 8k9 memory with coincidence drive in one half, anti-coincidence drive in the other.

Each type of stack can be delivered in two capacities: one in the maximum number of bits arrangement, the other in the current phased arrangement (of double the number of words and half the number of bits per word). Both versions are supplied with a two diode per line selection system. Capacities available are:

4k18 - 8k9
8k18 - 16k9
16k18 - 32k9

All the planar stacks are wired with a "bow tie" sense/inhibit wire. One sense/inhibit wire per bit is provided in the 4k and 8k capacities, and two for the 16k. The sense wire is split into two equal parts to allow simultaneous drive of the sense/inhibit line by two separate bit-drivers. Each sense/inhibit wire has four terminations; simplified sense/inhibit routeing, with its associated "worst pattern", is shown in Fig. 2. Each planar stack is provided with two current loops to facilitate the test procedure (one for the X drive, one for the Y drive - see Fig. 3). A thermistor can be added for drive current compensation.



Simplified wire diagram

1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1
1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1
1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1
1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1

Worst pattern

Fig. 2 Sense/inhibit line configuration
D = inhibit S = sense

Diode Selection

Diode packs, having 16 integrated diodes in each package, are used. Diode selection is based on a two diode per line system. The selection method for each type of stack is listed below, and Fig. 3 shows the principle of diode selection in the 4k18 - 8k9 stack.

stack capacity	X drive		Y drive	
	diode multiples of 2 diodes	line multiples of 8 lines	diode multiples of 2 diodes	line multiples of 8 lines
4k18	8	8	8	8
8k18	8	8	8	16
16k18	8	8	16	16

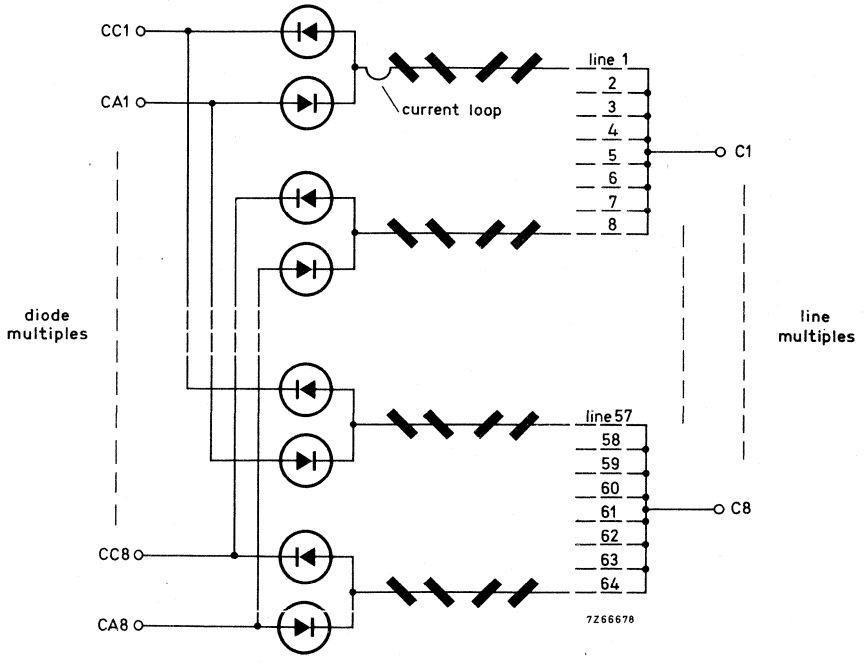


Fig. 3 Diode selection scheme for 4k18 and 8k9.
CC = common cathode, X or Y. CA = common anode, X or Y.
C = common X or Y.

Electrical Data

Cores used in the range of planar stacks are the 18 mil core-type 18H61. (Other 18 mil cores mentioned in this book can be used on request.) The operating conditions, at an ambient temperature of 25 °C, are listed below.

operating conditions	capacity			units
	4K18	8K18	16K18	
I_{nom}	640	640	640	mA
t_r	100	100	100	ns
t_d	300	300	300	ns
t_f	100	100	100	ns
rV_1	40	40	38	mV
t_p	160	165	170	ns
t_s	240	245	250	ns
R_x	5, 2	7, 8	17, 1	Ω
R_y	6, 3	7, 2	6, 6	Ω
$R_{s/z}$	2 x 4, 3	2 x 6, 4	2 x 12, 8	Ω
Load impedance S/Z	2 x 100	2 x 120	2 x 150	Ω

Interface

Planar stacks can be delivered with one of the following interface terminations:

1. Double-sided edge connector with contact pitches of 0, 1 inch.
2. Colour-coded cableform with twisted sense/inhibit wires.
3. Mini-wrap/solder pins with 0, 1 inch pitch.

Dimensions

Dimensions (in mm) of the various planar stacks are given in the table below.

stack capacity	with edge connector			cable form/mini wrap pins		
	length	width	height	length	width	height
4k18 - 8k9	147	163	12	153	170	12
8k18 - 16k9	190	196	12	190	187	12
16k18 - 32k9	250	215	12	240	215	12

PLANAR STACKS WITH 20 mil CORES

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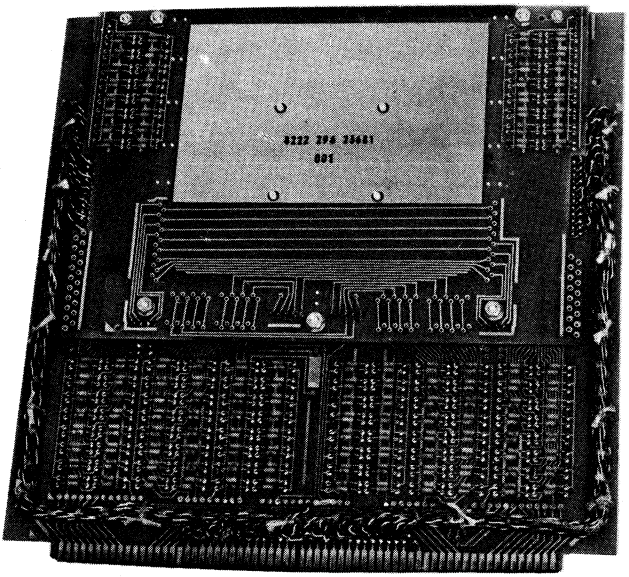


4k18 stack

Description

To be compatible with other matrix suppliers, our programme also includes a planar folded-construction stack with 20 mil cores in 4k18 - 8k9 capacities. The core material is type 20H89 but the other 20 mil (or 18 mil) cores mentioned in this book can be supplied on request. The stack is normally supplied with a 65-pole printed wiring connector (0,1 inch pitch - see photograph), but can also be supplied with cableforms or mini-wrap pins.

A two diode per line selection method is used. The bow-tie sense/inhibit wire is split for dual drive ; all four ends are accessible. Separate current loops are provided, one for X and one for Y drive, and an NTC thermistor is fitted for drive current compensation. Fig. 4 shows the simplified wiring diagram.

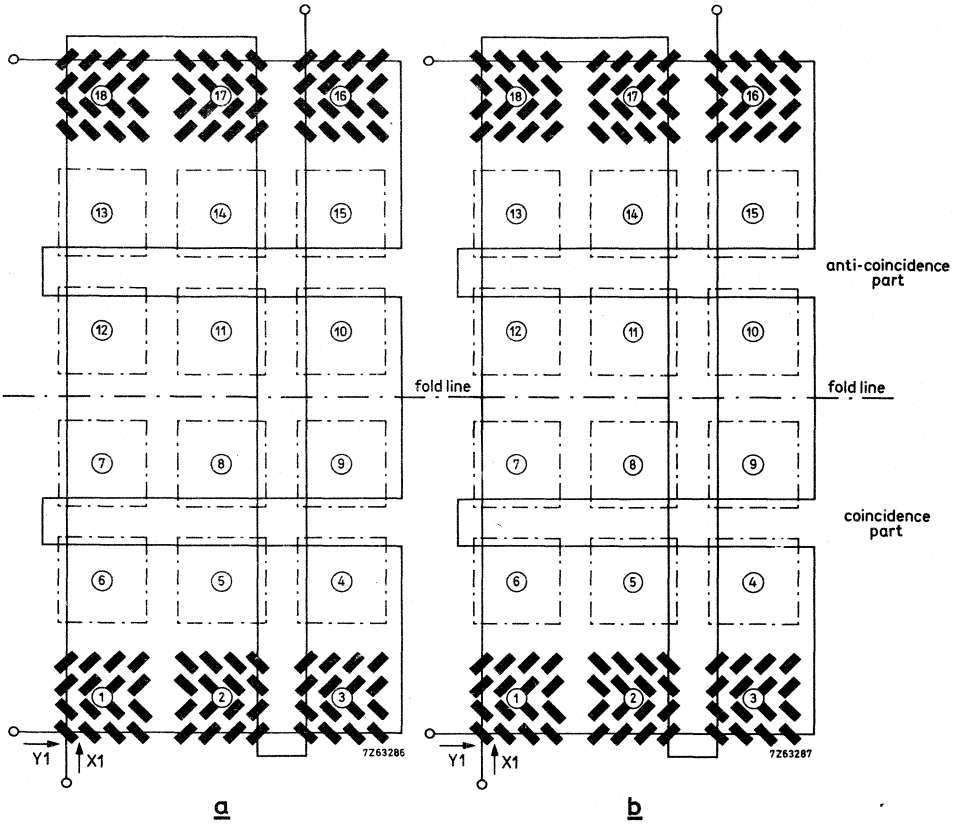


Fig. 4 Core arrays and X and Y line wiring scheme.
a. For 4k18 memory.
b. For 8k9 memory with coincidence drive in one half, anti-coincidence drive in the other.

Dimensions (in mm)

with p.w. connector			cable form/mini wrap pins		
length	width	height	length	width	height
209	203	8	190	178	8

3D/4-WIRE MATRICES AND STACKS
with 20 and 30 mil cores

MATRICES

These 3D/4-wire core matrices are wired directly onto a printed-wiring board and have the following features:

- the copper-clad surface of the printed-wiring board functions as a heatsink thereby reducing temperature differences in single planes;
- a rugged stack construction (9 mounting bolts);
- reduced stack height (the matrices are wired on both sides of the printed-wiring board.

Description

The core matrices are provided with a square-4 wired core-array on the top and bottom of a printed-wiring board. Wired core-arrays are secured to the copper cladding of the printed-wiring board by Dow Corning 630 lacquer. Four wires are strung through each core, these are the X, Y, Z and S wires. The X and Y wires run through the rows and columns of the core arrays. Wiring on top and bottom of the printed wiring board is interconnected through metallized-through holes.

Up to 4k each core array is supplied with one sense and one inhibit wire. 8k matrices have two sense and two inhibit wires; four sense and four inihibit wires are used in 16k matrices. The sense wire is wired diagonally through the core array; bifilar wiring through the rows and columns is used for the inhibit wire (Fig. 1). The sense wire is wired in such a way that disturbance voltages will cancel which results in a small common-mode signal.

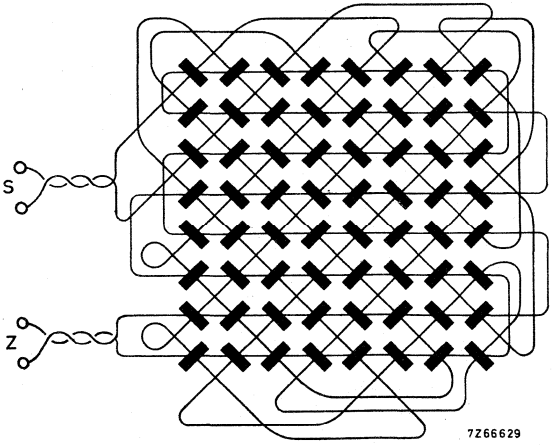


Fig. 1

Interlacing of the sense wires in two different core-arrays in 8k and 16k versions reduces the delta noise. The number of coupled cores per bit between the sense and inhibit wires is also decreased. The whole results in a better 1 and 0 discrimination.

Lacquering of the cores ensures a good heat transfer from the cores to the copper cladding; resistance to shock and vibration is increased.
The steep rise-time of the inhibit pulse may give rise to magnetic ringing in the cores but the lacquering has the effect of damping and therefore contributes to smaller cycle times. The dielectric constant of the lacquer produces a small disadvantage in that it decreases the characteristic impedance of the cores and increases the delay time slightly.
All preferred-range matrices are lacquered; unlacquered matrices can be supplied on request.

Available versions

Preferred matrices

20 mil matrices

p.w. board dimensions 115 x 115 mm

words	bits	core type	catalogue number
4k	8	20H92	2722 062 27001
4k	8	20H89	2722 062 27041
8k	4	20H92	2722 062 35001
8k	4	20H89	2722 062 35041
16k	2	20H92	2722 062 08001
16k	2	20H89	2722 062 08041

30 mil matrices

p.w. board dimensions 140 x 140 mm				p.w. board dimensions 90 x 90 mm			
words	bits	core type	catalogue number	words	bits	core type	catalogue number
4k	8	30F83	2722 061 27001	1k	8	30F83	2722 061 26001
8k	4	30F83	2722 061 35001	2k	4	30F83	2722 061 21001
16k	2	30F83	2722 061 08001				

3D/4-wire matrices on printed-wiring boards are only available with 20 mil or 30 mil cores. Other types of core material in these dimensions (from the range mentioned in this book) will be supplied on request.

Cross-over boards are available for matrices with more than 2 bits. These boards have printed interconnections for the X and Y drive wires on one side; wired core-arrays can be applied to the other side.

Example: A 4k/17 stack is composed of two 4k8 matrices and a cross-over plane with only one bit.

Note: 18 mil cores will not be used for 3D/4-wire matrices.

Sense /inhibit connections

Fig. A shows the location of the sense and inhibit terminations for the bits of the 20 mil and 30 mil 140 x 140 mm matrices: Fig. B shows similar detail for the 30 mil 90 x 90 mm matrices.

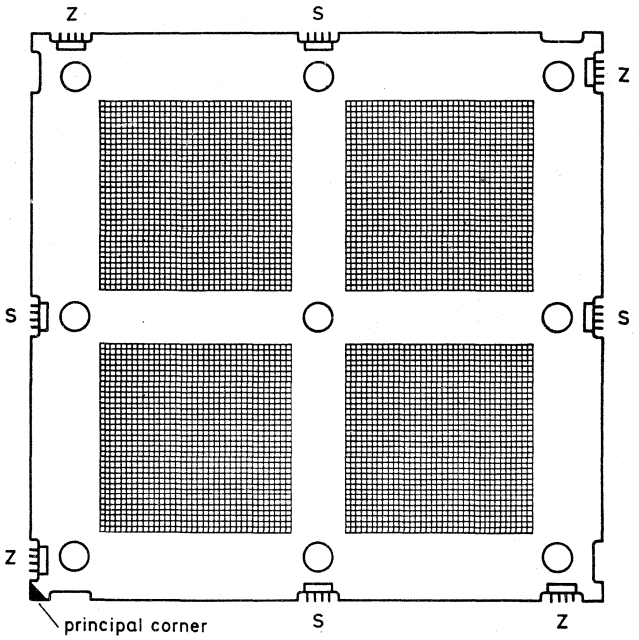


Fig. A

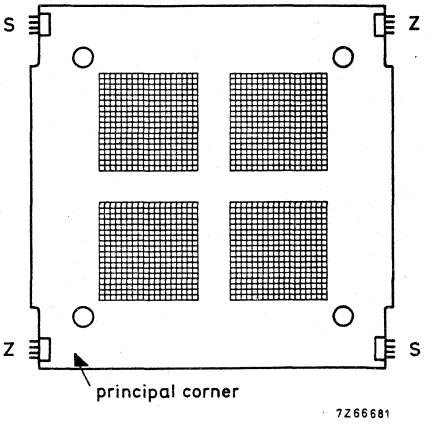


Fig. B

RZ 30942-1

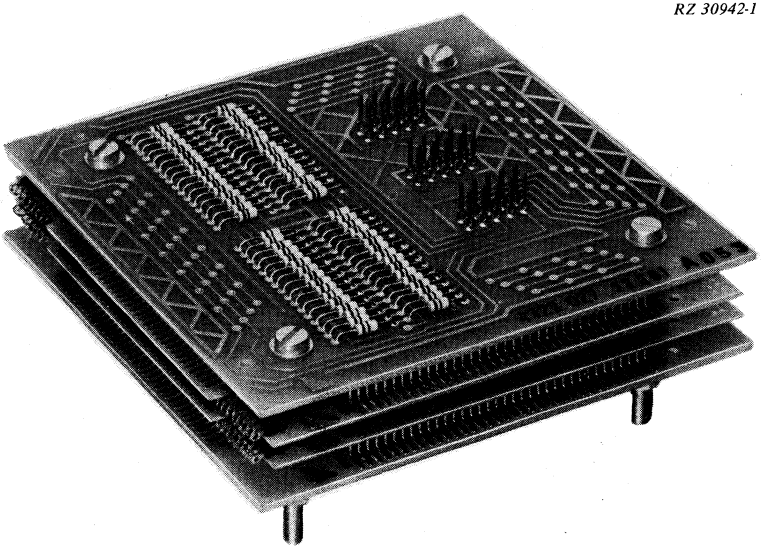


Photo 1 1k8 stack with 30 mil cores

RK 16009-4

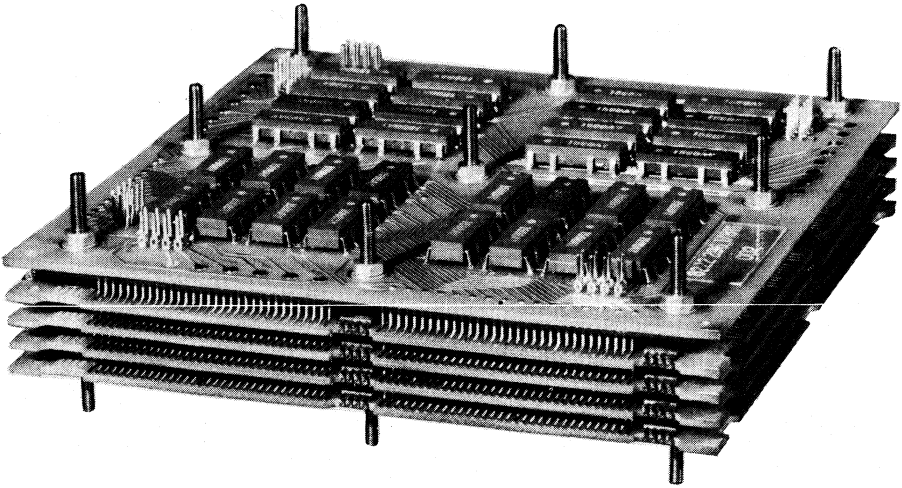


Photo 2 4k26 stack with 30 mil cores

MATRIX STACKS

The desired bit-capacity determines how many matrices must be stacked together. A turn-over board must be added to stacks built up with more than 2 bits per matrix board. A stack can be provided with a termination board or a diode board. Stacks with lead-off wires will be supplied on request. If heat-sinks are needed, stacks can be supplied with metal plates at both ends. Metal spacers between the printed-wiring boards and the 9 fixing bolts guarantee good heat conduction from stack to heat-sinks.

Comb type contact springs provide the interconnections needed for the drive wires in the stack. On a termination board the drive wires end in mini-wrap pins (see Photo 2). These pins are arranged to enable the 10-pole connector type 4322 026 83980 to be used.

Stacks with diode boards employ BAV10 diodes at 2 diodes per line (see Photo 1 and Survey of diode selection). The diode board is provided with mini-wrap pins arranged so that connector type 4322 026 83980 can be used (except 4k version).

Rigid construction, and the lacquering of wires and cores to the matrix board, make each stack highly resistant to vibration damage. Memory stacks comply fully with the mechanical requirements of MIL STD 202C.

RK 16009-2

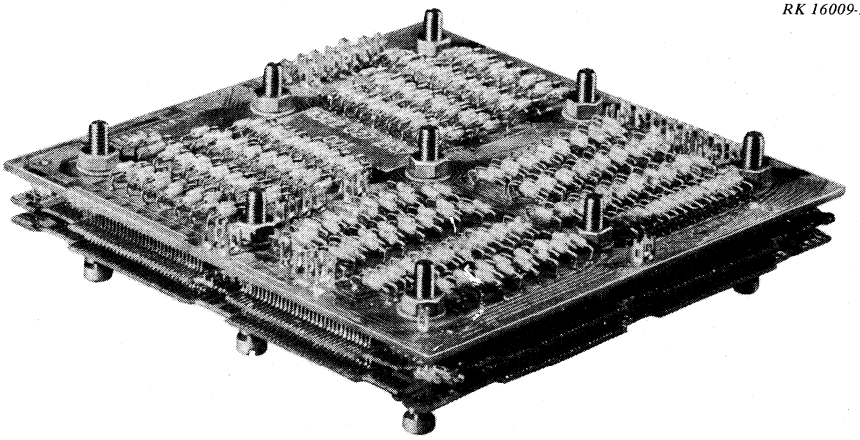


Photo 3 4k12 stack with 20 mil cores

Survey of diode selection

word capacity	X drive		Y drive	
	multiples of 2 diodes	line multiples	multiples of 2 diodes	line multiples
1k	4	8 of 4 lines	4	8 of 4 lines
2k	8	8 of 4 lines	8	8 of 8 lines
4k	8	8 of 8 lines	8	8 of 8 lines
8k	8	8 of 8 lines	8	8 of 16 lines
16k	8	8 of 16 lines	8	8 of 16 lines

20 mil Stacks (Photo 3)

Diode boards for 20 mil stacks use single diodes type BAV10. The 4k matrix stack has one diode board mounted on the top, and the 8k and 16k matrix stacks have two diode boards mounted one on top and bottom.

A dimensional drawing is shown in Fig. 1

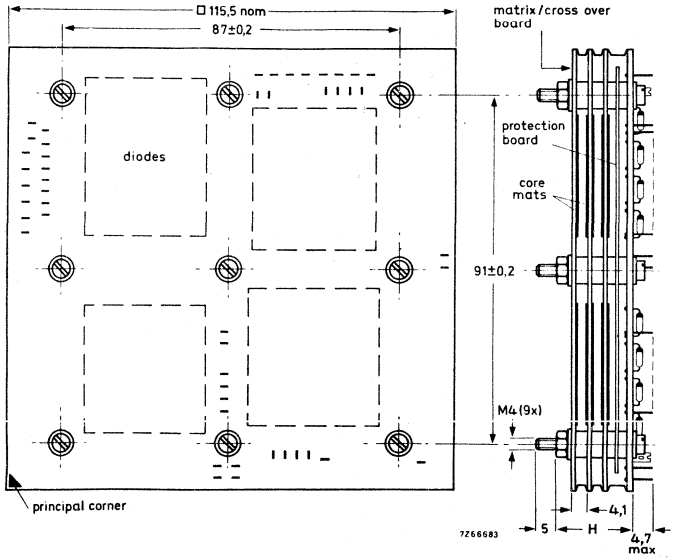


Fig. 1 Height of 4k stack $H_{nom} = n \cdot 4,1 + 11,5$ mm
of 8k and 16k stack $H_{nom} = (n-1) \cdot 4,1 + 23$ mm

n = number of matrices

30 mil Stacks

Two types of 30 mil stacks are available, one type for 1k and 2k matrices (Fig. 2, Photo 1) and one type for 4k, 8k and 16k matrices (Fig. 3, Photo 2). Stacks with 1k and 2k matrices use diode boards having single diodes BAV10 as opposed to the stacks with 4k, 8k and 16k matrices which use diode boards having diode packs BAV40 (each of which contains eight BAV10 diodes). The 1k and 4k matrix stacks use one diode board mounted on top of the stack (see photographs); the 2k, 8k and 16k matrix stacks use two diode boards (mounted one on top and bottom). Dimensional drawings of the 1k and 4k stacks are shown below.

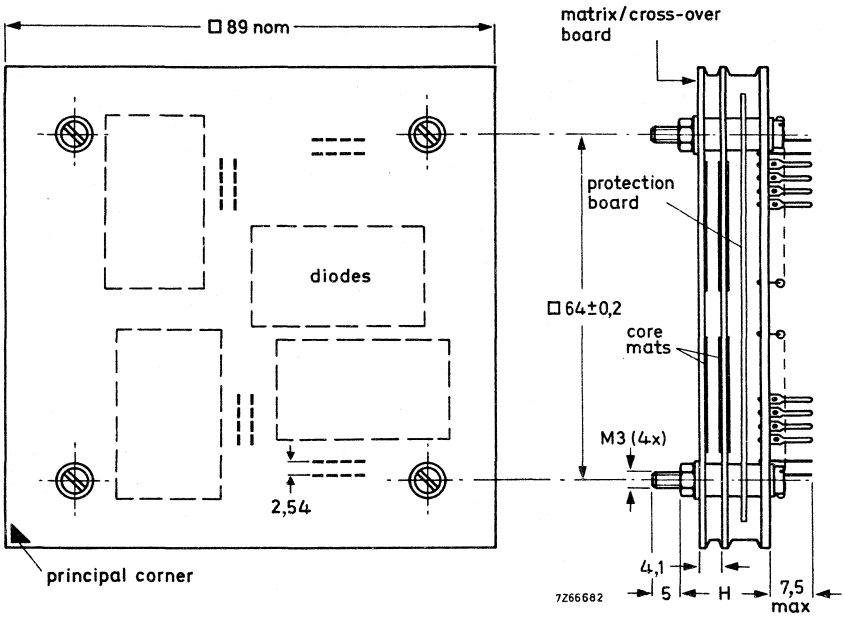


Fig. 2 Height of 1k stack $H_{nom} = n \cdot 4,1 + 10,5$ mm
of 2k stack $H_{nom} = (n-1) \cdot 4,1 + 23,5$ mm

n = number of matrices

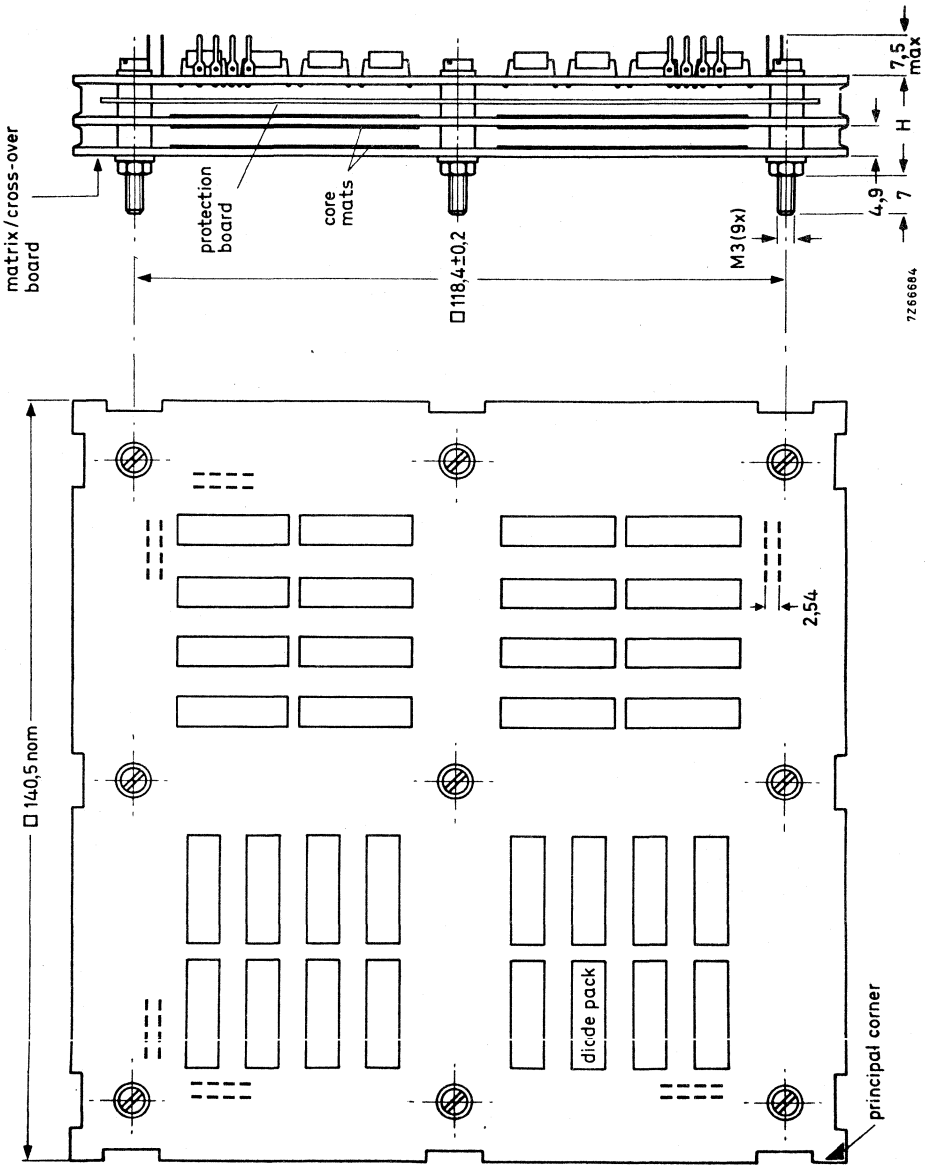
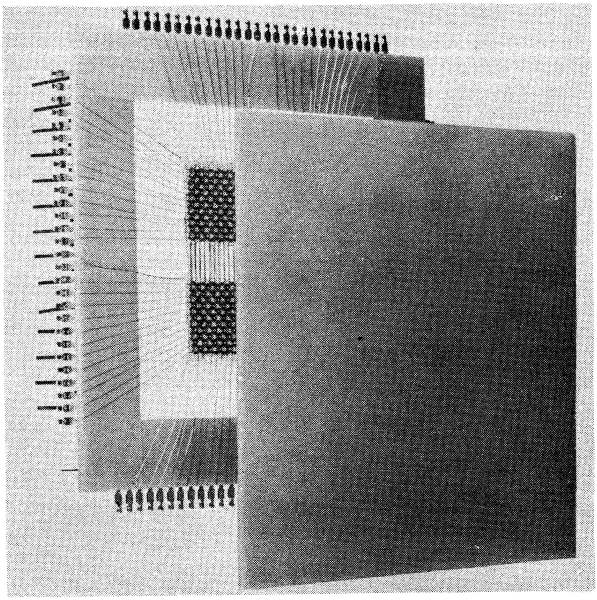


Fig. 3 Height of 4k stack $H_{nom} = n \cdot 4,9 + 12$ mm
of 8k and 16k stack $H_{nom} = (n-1) \cdot 4,9 + 25$ mm

n = number of matrices

PLATRICES AND STACKS WITH 50 mil CORES

RZ 21192-2



PLATRICES

Platrices are matrix planes that can be mounted directly onto a printed-wiring board. They are designed for use in desk-size book-keeping machines, desk calculators, invoicing machines, cash registers, and also in other applications such as machine tool equipment and measuring apparatus.

The wiring of the cores is based on the coincident current (M.I.T.) system. The platrices are supplied with 50 mil cores type 50C82, which enables them to operate within the temperature range of 10 to 70 °C without temperature compensation. As the X, Y and Z wires run through each core twice (halving the drive currents) relatively simple drive circuits can be used.

CONSTRUCTION

Platrices consist of a frame and terminals, the matrix and a protection plate. Cores and wiring are coated with silicon-rubber, by which means a very ruggid construction is obtained. Frames and plates are made from a paper-based laminate to standardised dimensions.
The frame consist of four pairs of strips, glued together, which hold the terminals in between. The terminals are L-shaped, forming single rows of soldering tags horizontally and double rows of pins vertically. The ends of the matrix wires are wrapped around the tags and then dip-soldered. See detail, Fig. 1.

The rows of pins are destined for mounting in a printed-wiring board. The distances between adjacent pins in a row and between adjacent rows are 5.08 mm, adjacent rows are shifted by 2, 54 mm with respect to each other. Therefore platrices can be mounted on a printed-wiring board with a grid of 2, 54 mm pitch. Before one platrix is stacked on another, all pins are cut-off.

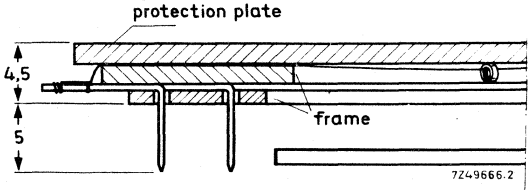


Fig. 1 Detail

Stacks of maximum four platrices with series connected drive wires can be supplied. All drive lines are available on the bottom plane to allow the stack to be mounted on a printed-wiring board.

Since the number of soldering pins determines the mechanical dimensions of the platrix (see photograph) these dimensions are reduced if the number of pins is reduced. Our 122 x 122 mm platrices have proved to be too large in practice. They are now wired on a frame of 102 x 102 mm achieved by interconnecting the drive wires *).

As a result of using this method two platrix versions are now available:

Version A These are our conventional platrices which can be stacked because all "X" and "Y" drive wires are accessible separately (see Fig. 2).
Also in version A are the new types of fourfold platrices with interconnected drive wires and reduced dimensions, 4 x 10 x 10 mm, 4 x 16 x 16 mm and 4 x 20 x 20 mm.

Version B Single and two-fold platrices of version A can be supplied with reduced dimensions by the interconnecting of the drive wires. These version B platrices cannot be stacked, because not all drive wires are separately accessible.

*) Other types of platrices with reduced dimensions can be supplied on request.

STANDARD RANGE OF PLATRICES , catalogue number 2722 051 .....
suffix

VERSION A			VERSION B		
core pattern	catal. nr. suffix	dimensions (mm)	core pattern	catal. nr. suffix	dimensions (mm)
16 x 16	02051	82 x 82			
4 x 8 x 8	22051	82 x 82	32 x 32	05081	102 x 102
4 x 4 x 16	28051	82 x 82	2 x 16 x 32	20081	102 x 102
4 x 10 x 10	04001	82 x 82			
18 x 24	03001	82 x 82			
16 x 32	10051	82 x 122			
4 x 8 x 16	29051	82 x 122			
4 x 12 x 12	24051	102 x 102			
32 x 32	05051 *)	122 x 122			
2 x 16 x 32	20051 *)	122 x 122			
4 x 16 x 16	25081	102 x 102			
4 x 16 x 16	25051 *)	122 x 122			
4 x 20 x 20	09001	102 x 102			

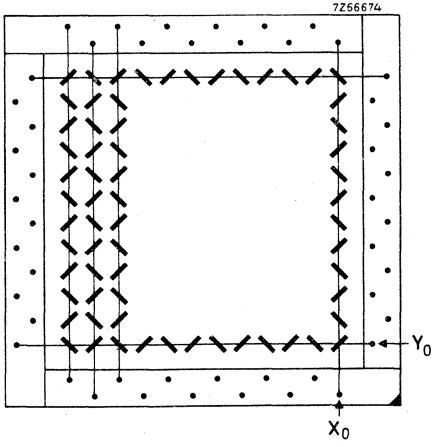


Fig. 2 Simplified diagram of a conventional platrix with a single core mat (version A).

*) For post deliveries only.

Platrices with four-fold core mat (version A)

In four-fold core mats the four bits must be switched simultaneously. One half of the X drive wire must be interconnected with the other half, and the Y drive wires are treated similarly. These interconnections are made externally on several of our standard platrices.
The number of soldering tags can be reduced by a factor 2 if the interconnections of drive wires are made with continuous wiring (see Fig. 3). This method is applied in our new platrices 4 x 16 x 16 and 4 x 20 x 20, which are now wired on a frame of 102 x 102 mm, giving a space reduction of 30%.

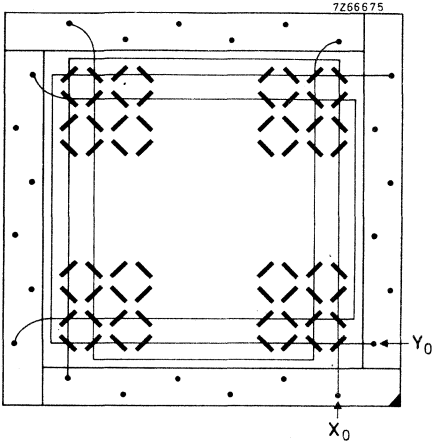


Fig. 3 Simplified diagram of a platrix with 4-fold core mat (version A).

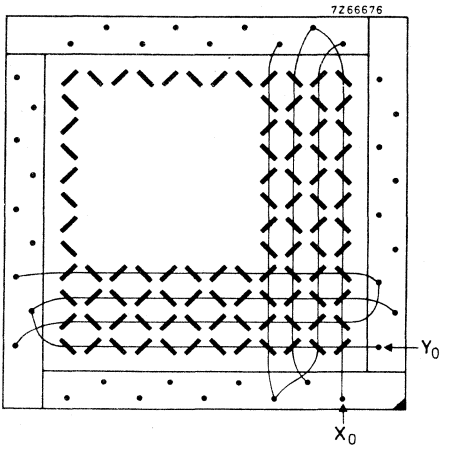


Fig. 4 Simplified diagram of a platrix with a single core mat (version B).

Platrices with a single core mat (version B)

In platrices with only one core array, the "X" and "Y" drive wires are each interconnected at one end (see Fig. 4), odd wires at one side, even wires at the other.
Only three soldering tags are needed for two drive wires, i.e. for the 32 x 32 platrix, 24 drive-wire tags are used at each side of the platrix: 8 of these are common.
A 32 x 32 platrix wired in this manner fits a 102 x 102 mm frame.

Note:

In single core mats the inhibit wire can be omitted making them cheaper.

Platrices with two-fold core mat

In the two-fold core mats two bits are switched simultaneously. Therefore the two halves of the "X"-wires must be interconnected. This is done by continuous wiring in the platrix.
The "Y" wires are interconnected at one end as in single core mats (see Fig. 5).

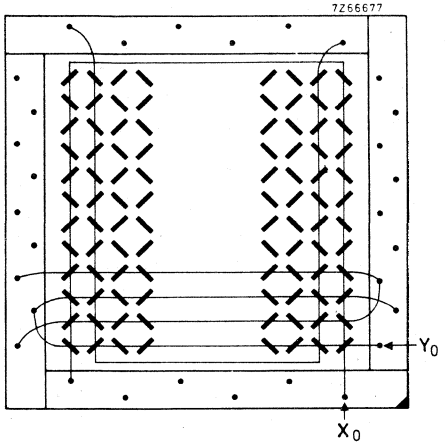


Fig. 5 Simplified diagram of a platrix with a two-fold core mat (version B).

As can be seen from Fig. 5 this version is an intermediate form of the four-fold and single core mats of Figs. 3 and 4. This system of wiring enables the 2 x 16 x 32 platrix to fit a 102 x 102 mm frame.

ELECTRICAL DATA

Cores and wiring

The Platrices are provided with type 6C2 cores, which have a low temperature coefficient. To reduce the drive current by a factor two, the "X", "Y" and "Z" wires are wired twice through each core. The sense wire is single. See the wiring diagrams.

Nominal conditions

Drive currents I_x, I_y, I_z	
amplitude	185 mA
pulse rise time	0.3-0.6 μs
pulse duration	1.2 μs
Strobe time for "1" output	0.45-0.75 μs
Ambient temperature	10-70 °C

Recommended load impedance of sense wire: 115 Ω in parallel with 100 pF.
To obtain a favourable one-zero ratio the pulse rise time must be chosen as low as possible.

Typical response

Output "1" signal during strobe time	35 mV
Output "0" signal during strobe time in worst pattern	2 mV
Switching time	1.3-1.6 μs

Test conditions

Each core in the Platrix is tested on the "one" output signal, with marginal drive currents, disturb ratio 0.61. The Platrices meet the MIL specifications STD 202.

Drive current	I_x	I_y	I_z	
amplitude	170	170	200	mA
pulse rise time	0.3	0.3	0.3	μs
pulse duration	1.5	1.5	2	μs
Strobe time for "1" output	0.45-0.75			μs
Ambient temperature	10-70			°C

Worst pattern

	1	1	0	0
	0	0	1	1
principal	0	0	1	1
corner	1	1	0	0

Accepted limits (at test conditions)

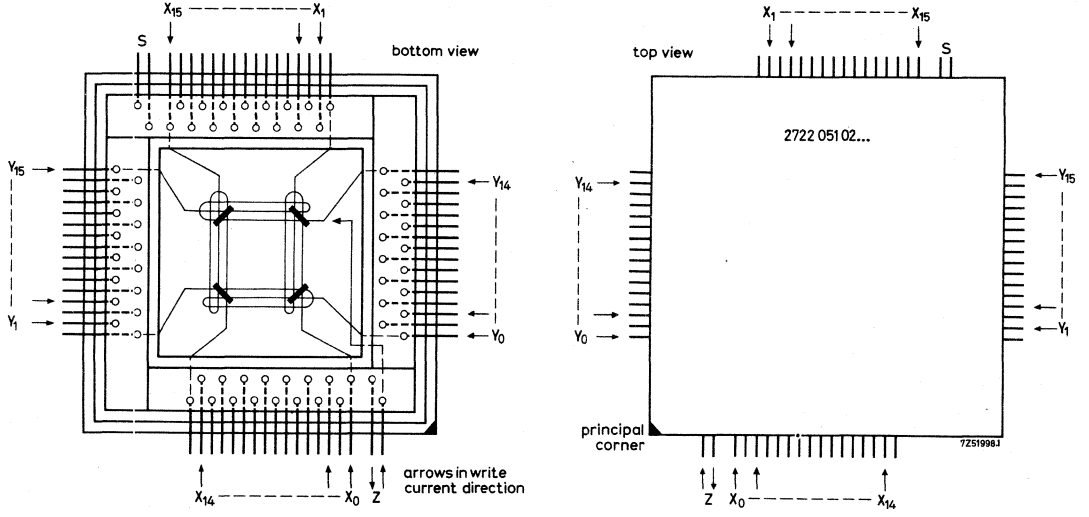
Output "1" signal during strobe time	≥ 25 mV
Output "0" signal during strobe time in worst pattern	≤ 3 mV
Switching time	$\leq 1.4\ \mu$s
Insulation resistance	≥ 100 MΩ
Maximum permissible interwinding voltage	80 V

STACKS

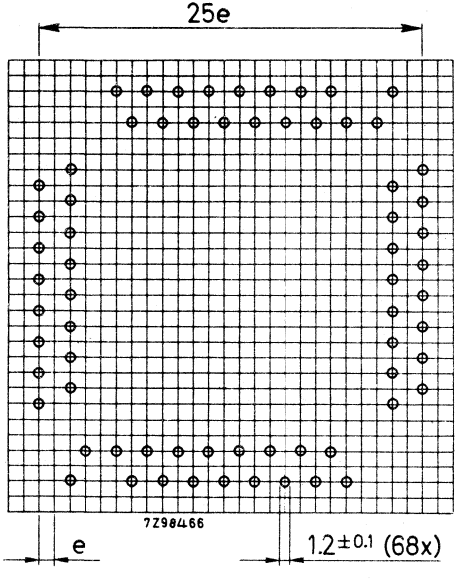
Stacks of maximum 4 standard Platrices having series-connected drive wires can be supplied. The stacks can be mounted direct on a printed-wiring board which possesses all tracks necessary for the ingoing and outgoing X and Y-drive currents, as well as tracks for the S and Z wires of the lowest plane.

CONNECTIONS AND HOLE PATTERNS

16 x 16



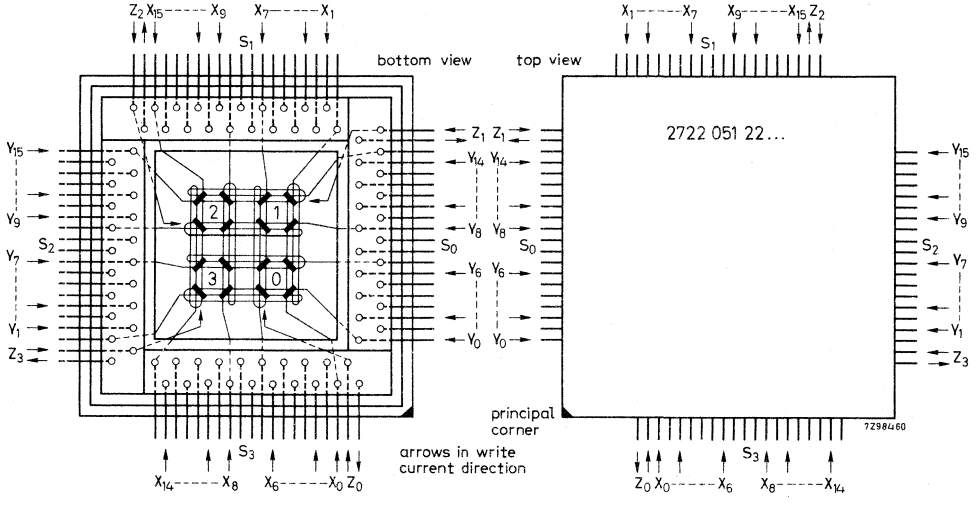
Platrix 16 x 16



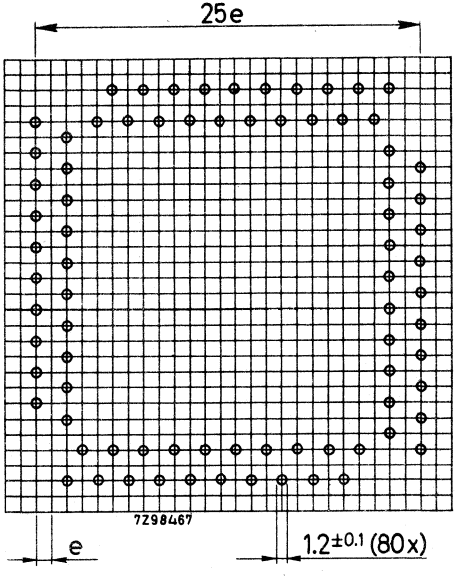
Component side.

Hole pattern for Platrix 16 x 16
e = 2.54 mm

4 x 8 x 8

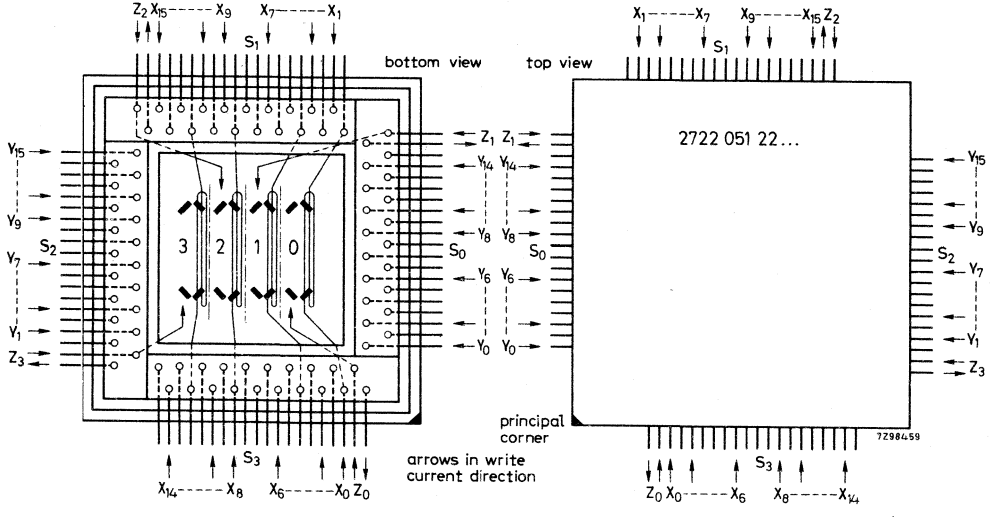


Platrix 4 x 8 x 8

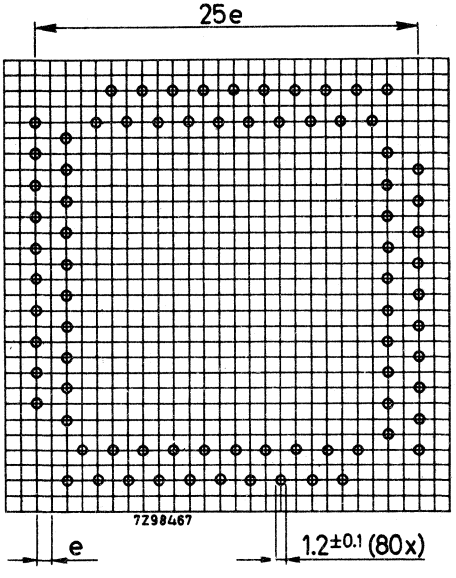


Hole pattern for Platrix 4 x 8 x 8
e = 2.54 mm
Component side.

4 x 4 x 16



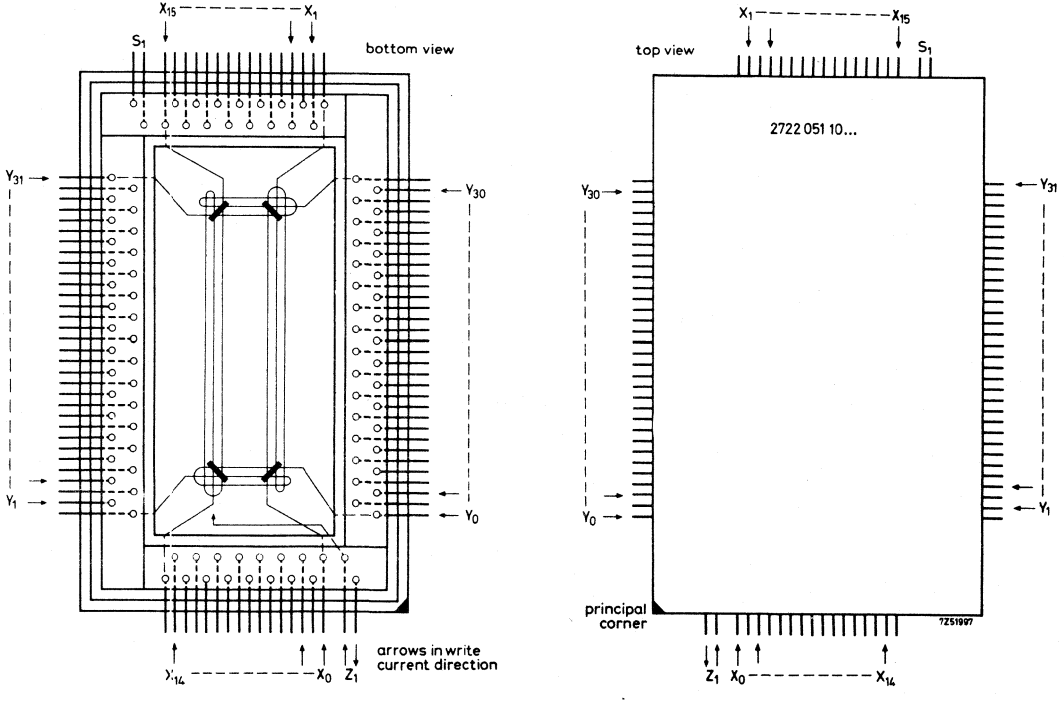
Platrix 4 x 4 x 16



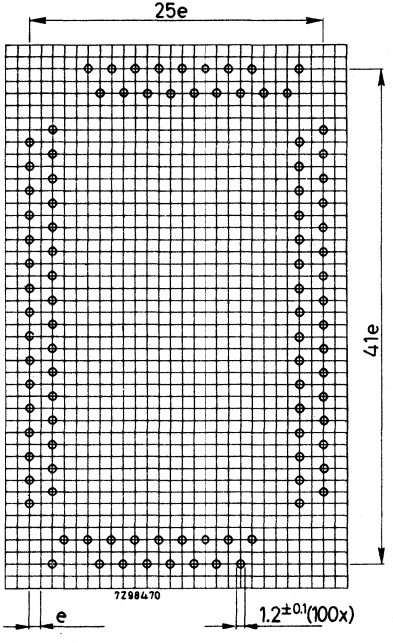
Component side.

Hole pattern for Platrix 4 x 4 x 16
e = 2.54 mm

16 x 32



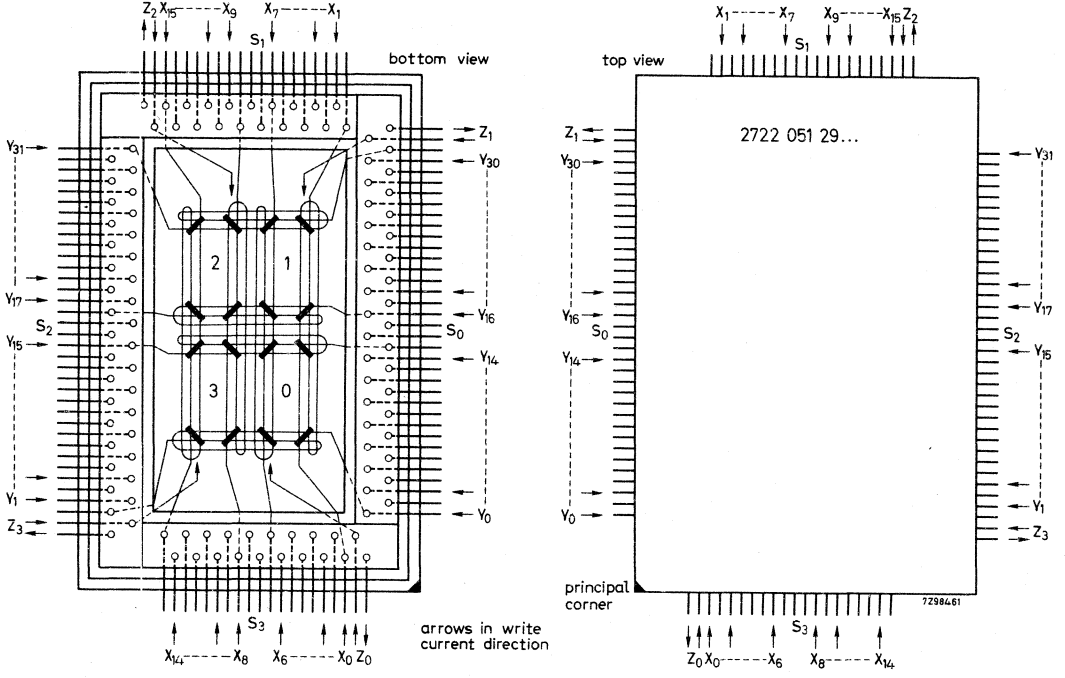
Platrix 16 x 32



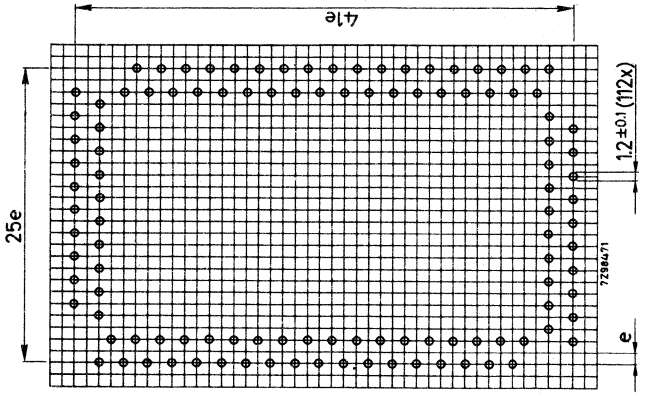
Component side.

Hole pattern for Platrix 16 x 32
e = 2.54 mm

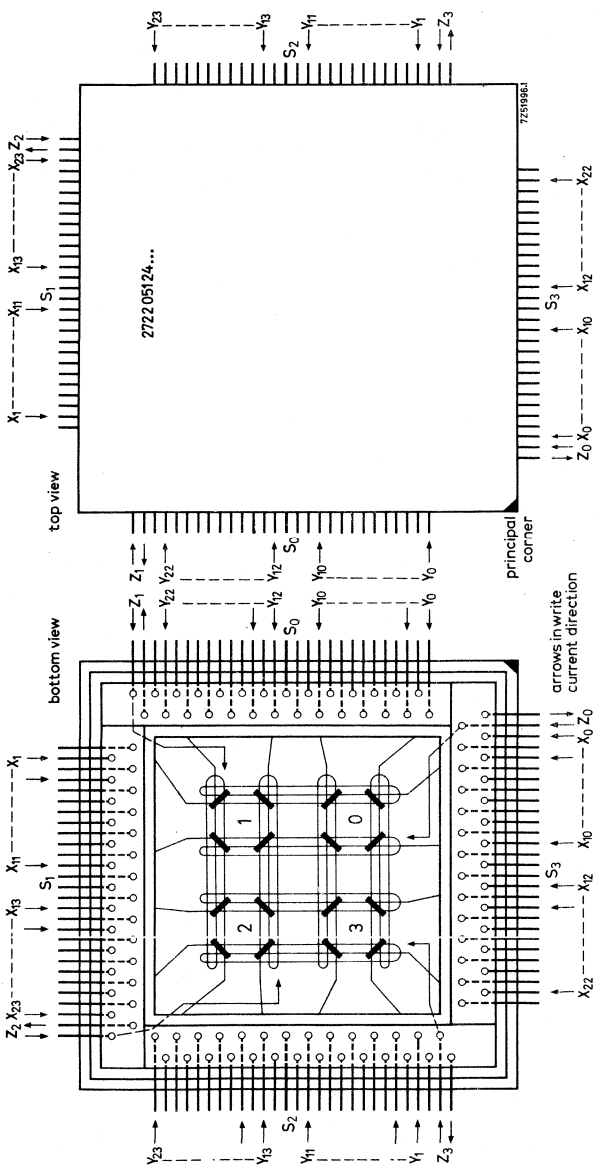
4 x 8 x 16



Platrix 4 x 8 x 16

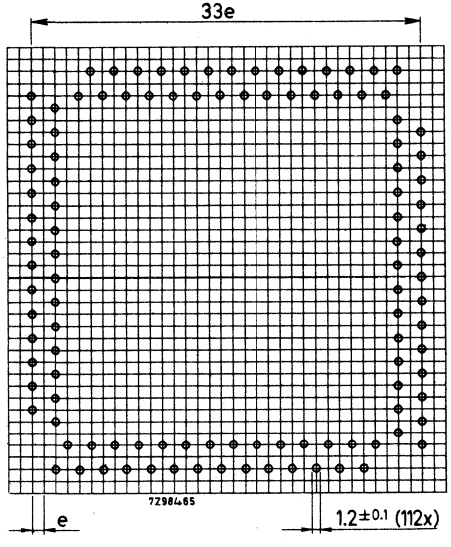


Hole pattern for Platrix 4 x 8 x 16
e = 2.54 mm
Component side.



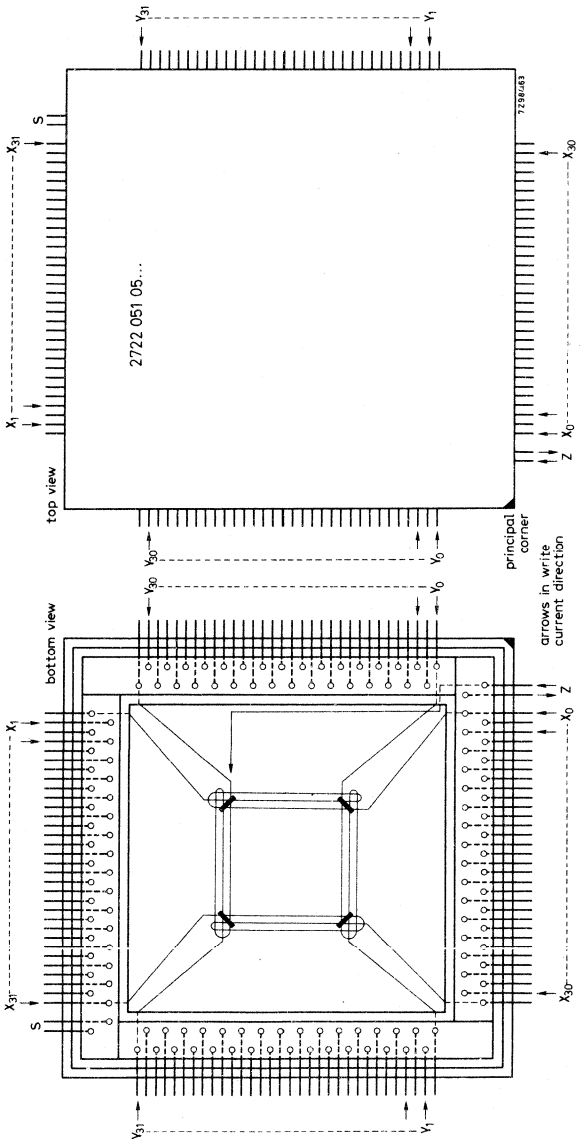
Platrix 4 x 12 x 12

± x 12 x 12



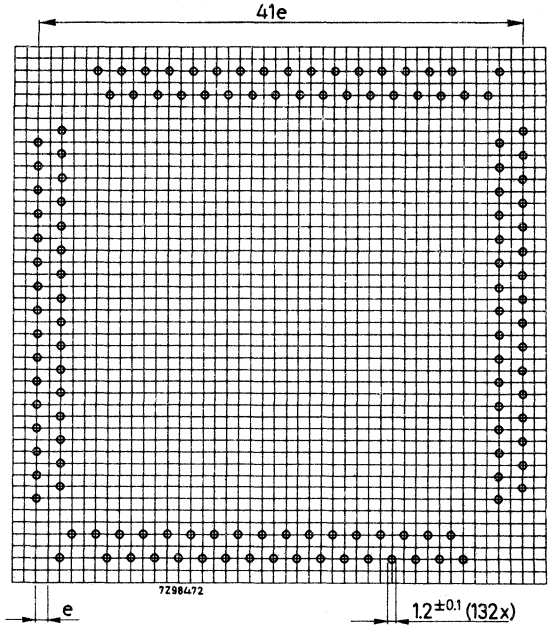
Component side.

Hole pattern for Platrix 4 x 12 x 12
e = 2.54 mm



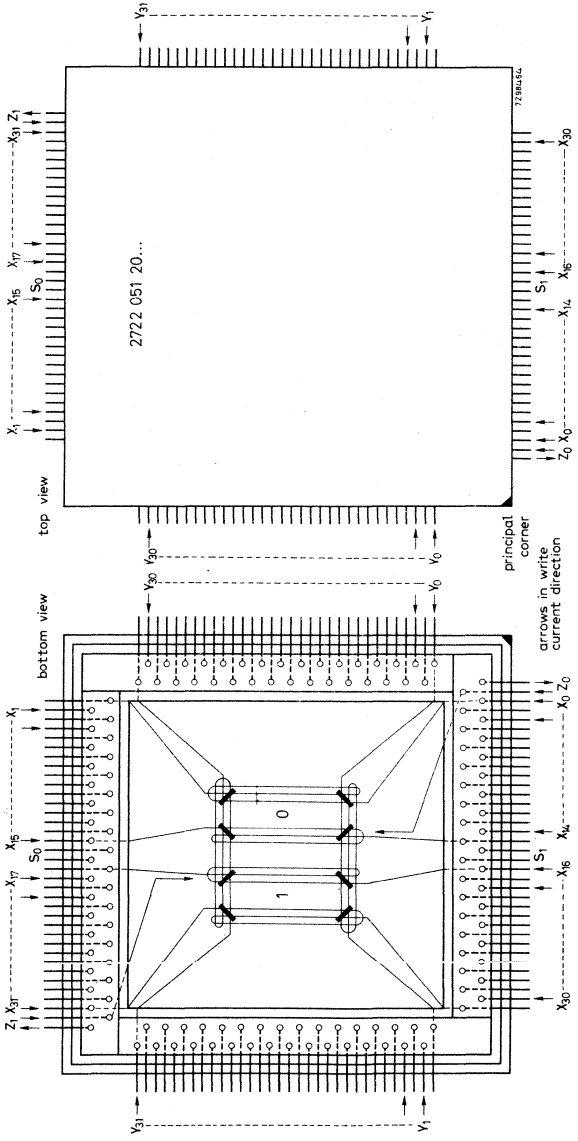
Platrix 32 x 32

32 x 32



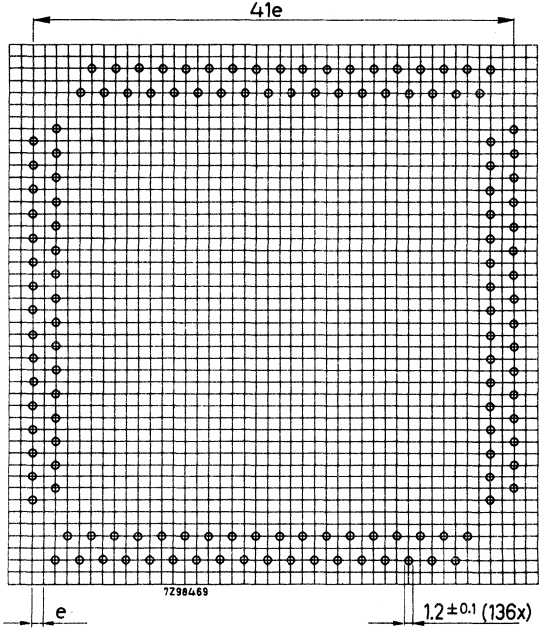
Component side.

Hole pattern for Platrix 32 x 32
e = 2.54 mm



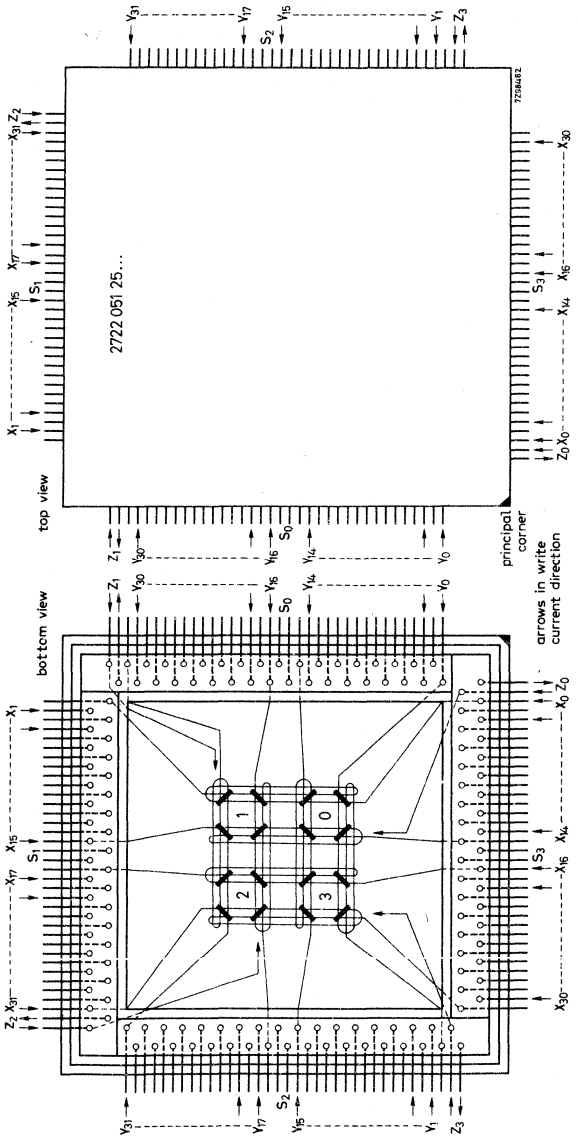
Platrix 2 x 16 x 32

2 x 16 x 32



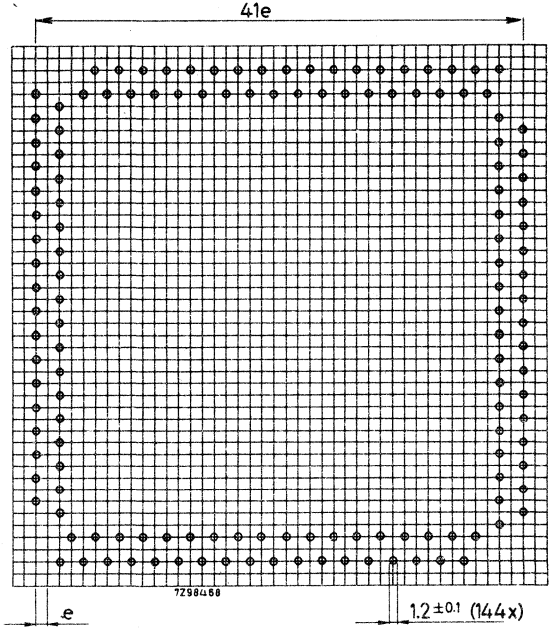
Component side.

Hole pattern for Platrix 2 x 16 x 32
e = 2.54 mm



Platrix 4 x 16 x 16

4 x 16 x 16



Component side.

Hole pattern for Platrix 4 x 16 x 16
e = 2.54 mm

Core memory systems

INTRODUCTION

A magnetic core memory is an equipment for the storage of digital information and can be used e.g. in data handling, process control, machine tool control, stock control, traffic control systems, nuclear energy analysis, instrumentation and electronic telephone exchanges.

Our magnetic core memories are complete memories consisting of digital circuit blocks and a ferrite core matrix stack which are assembled in units for standard mounting methods.

Their production is based on a long experience in mass production of ferrite memory cores, matrices and stacks as well as circuit blocks. Therefore they offer an economical and highly reliable contribution to their application fields.

The high reliability is specially due to:

- Worst-case design of all circuits, where calculations have been performed with end of life data of all components.
- Professional semiconductors being used throughout.
- Severe control procedure of all components and sub-assemblies, before, during and after the whole production process.
- Testing of the complete memory under severe circumstances:

  1. extreme voltage tolerances
  2. extreme temperatures
  3. worst-pattern test programme for checking the margins of the memories.

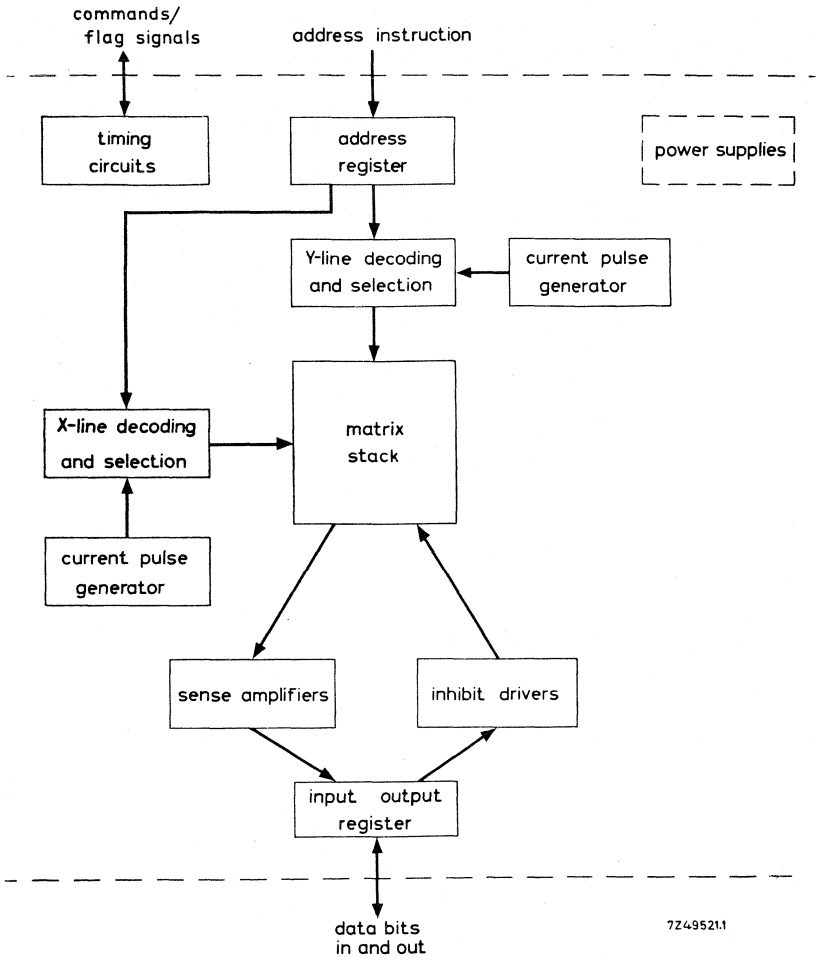
In our memory systems use is made of plug-in printed circuit boards to mount all the circuitry.

→ SELECTION GUIDE

capacity	memory type		cycle time	access time
256/4	FI-11 FI-12	maintenance types *)	6 µs	1 µs
256/18	FI-14		20 µs	1 µs
1 k/8	FI-2		4 µs	0,6 µs
1 k/8	FI-22		1,2 µs	0,28 µs
1 K/13	FI-26		1 µs	0,5 µs
4 k/8 8 k/8 16 k/8	FI-128 FI-138 FI-148	FI-100	1,5 µs	0,5 µs
4 k/18 (16, 12)	FI-75		0,75 µs	0,3 µs
8 k/16	FI-1316		1,2 µs	0,45 µs
16 k/16	FI-1416		1,2 µs	0,46 µs
8 k/18	FI-68		0,65 µs	0,26 µs
16 k/18	FI-69		0,7 µs	0,3 µs
4 k-16 k/12-36	PRM-7		0,75 µs	0,3 µs
16 k/36	Q14		1,4 µs	0,6 µs

*) Not included in this Handbook; information will be supplied on request.

BLOCK DIAGRAM OF THE COMPLETE MEMORIES



SOME DEFINITIONS

Cycle time : the minimum time between two successive cycle start pulses.

Access time : the time interval between receiving a cycle start pulse and the stored output becoming available.

1,2 µs CORE MEMORY SYSTEM

QUICK REFERENCE DATA	
Capacity	1 k/8
Cycle time	1,2 µs
Access time	0,28 µs
Selection bits for easy paralleling	
Data input/output register	
TTL compatible	
Random access	

DESCRIPTION

A 3D, 3 wire complete random access core memory system equipped with 18 mil cores, built on one printed-wiring board. The electrical and physical properties make this memory system in particular suitable for use in small office machines, desk calculators, measuring equipment and industrial control applications.

MECHANICAL DATA

Dimensions

width	21 mm
height	208 mm
depth	197 mm

Mounting

The components are mounted on a glass epoxy printed-wiring board, which is provided with a 64-pins interface connector F054.

ENVIRONMENTAL DATA

Ambient temperature range,	operating	0 to +55 °C
	non-operating	−40 to +75 °C
Humidity		up to 90% (without condensation)
Shock		1000 bumps of 10 g
Vibration		5 to 150 Hz at 5 g max.
Cooling		by natural convection of air

ELECTRICAL DATA

Memory capacity

number of words	number of bits/word
1024	8

→ Memory speed (see also timing diagrams)

mode of operation		cycle time	access time
read/restore	full cycle	1,2 µs	0,28 µs
clear/write	full cycle	1,2 µs	
read/modify/write	split cycle	1,2 µs	0,28 µs
clear/write	split cycle	1,2 µs	

Input signals

P_{st} start command; initiates either a read/restore or clear/write full cycle, or a read- or clear-part of a split cycle.
P_{w} write command; initiates the write part of a split cycle.
L_{hc} full/split cycle level; determines either a full- or split cycle operation mode.
L_{cl} clear level; determines either a clear or a read operation.
$L_{sb\ n}$ selection bit levels (n = 1, 2); both levels must be logic 1 or 0 for duration of P_{st} or P_{w}.
$L_{ab\ n}$ address information (n = 0...9)
$L_{wbi\ n}$ data input (n = 1...8)

Output signals

$L_{wbo\ n}$ data output (n = 1...8)

Interface

Input and output levels "1" HIGH TTL level
"0" LOW TTL level

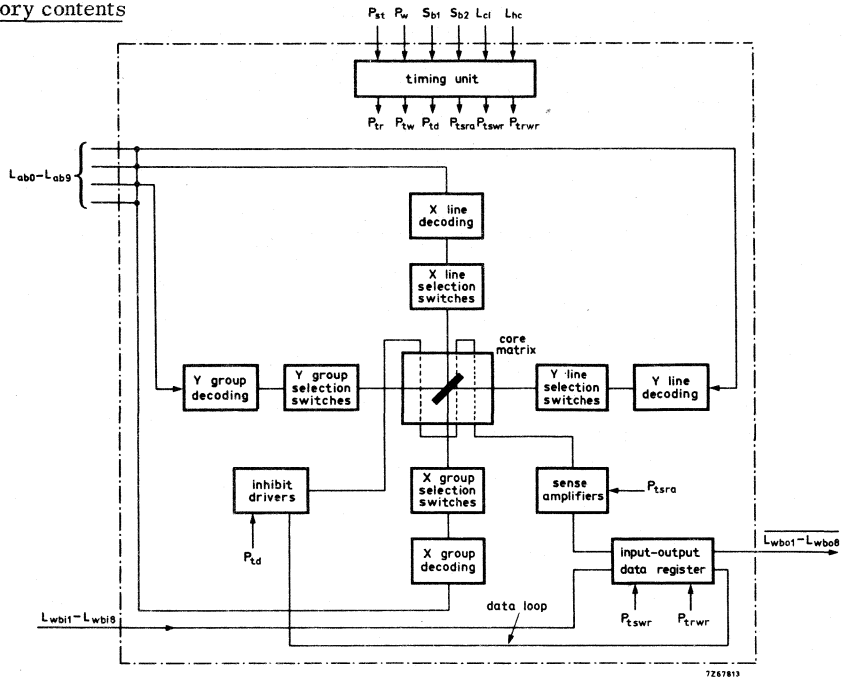
The output signals are generated by an open collector (SN7438); maximum "1" voltage is 5,5 V. Sink capability of output stages equals to 40 mA.
Interface connections are made via a 2,54 mm (0,1 in) pitch two-part printed-wiring connector F054, fitted to the 208 mm side of the printed-wiring board.

Power supply requirements

supply voltage	current consumption	
	stand-by	operating
→ +5 V, ± 5%	1 A	max. 2,5 A
→ -5 V, ± 5%	0,1 A	max. 0,1 A

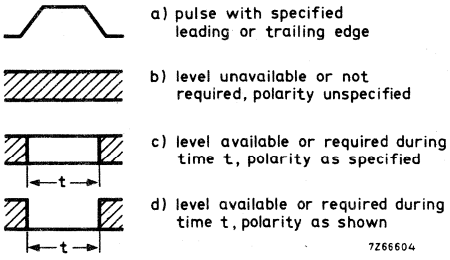
Note - The current values are valid for operation at worst case conditions.

Memory contents

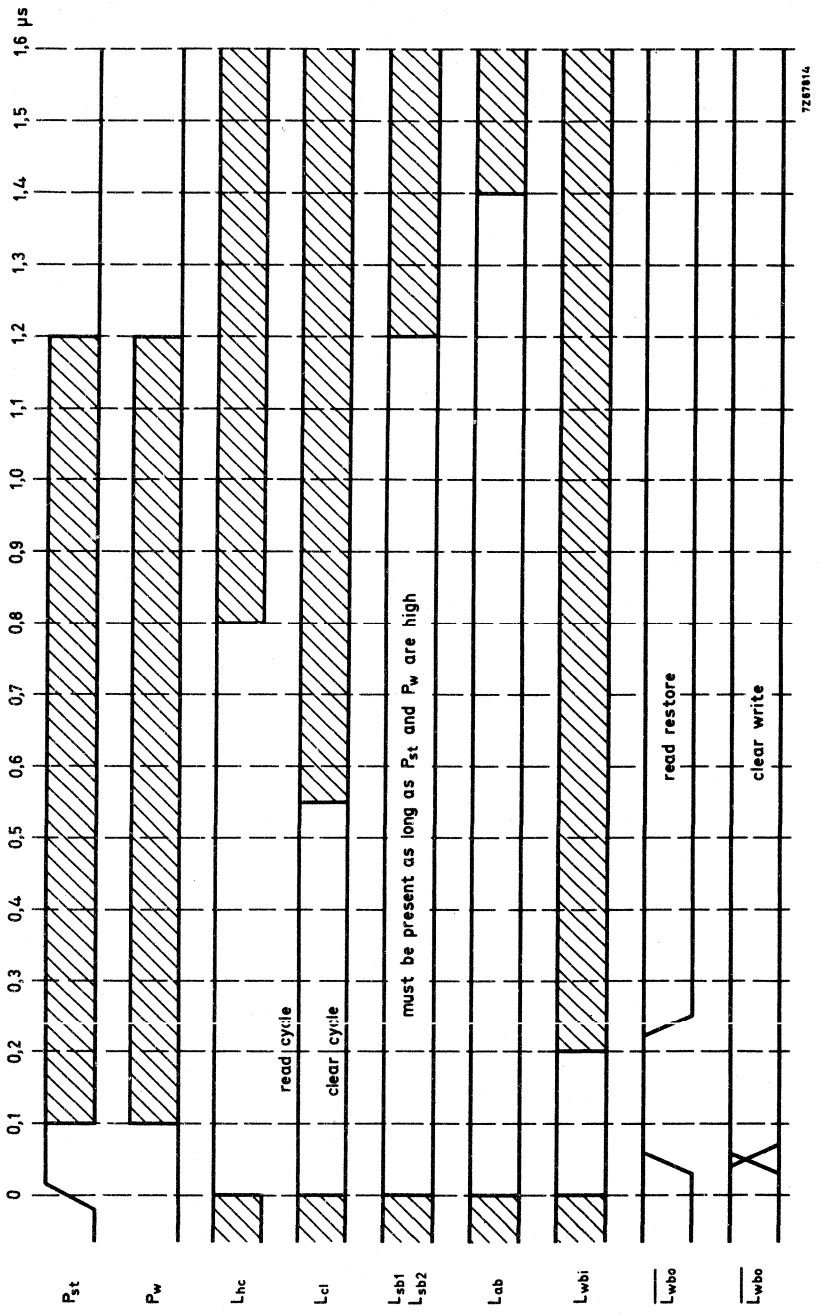


Block diagram

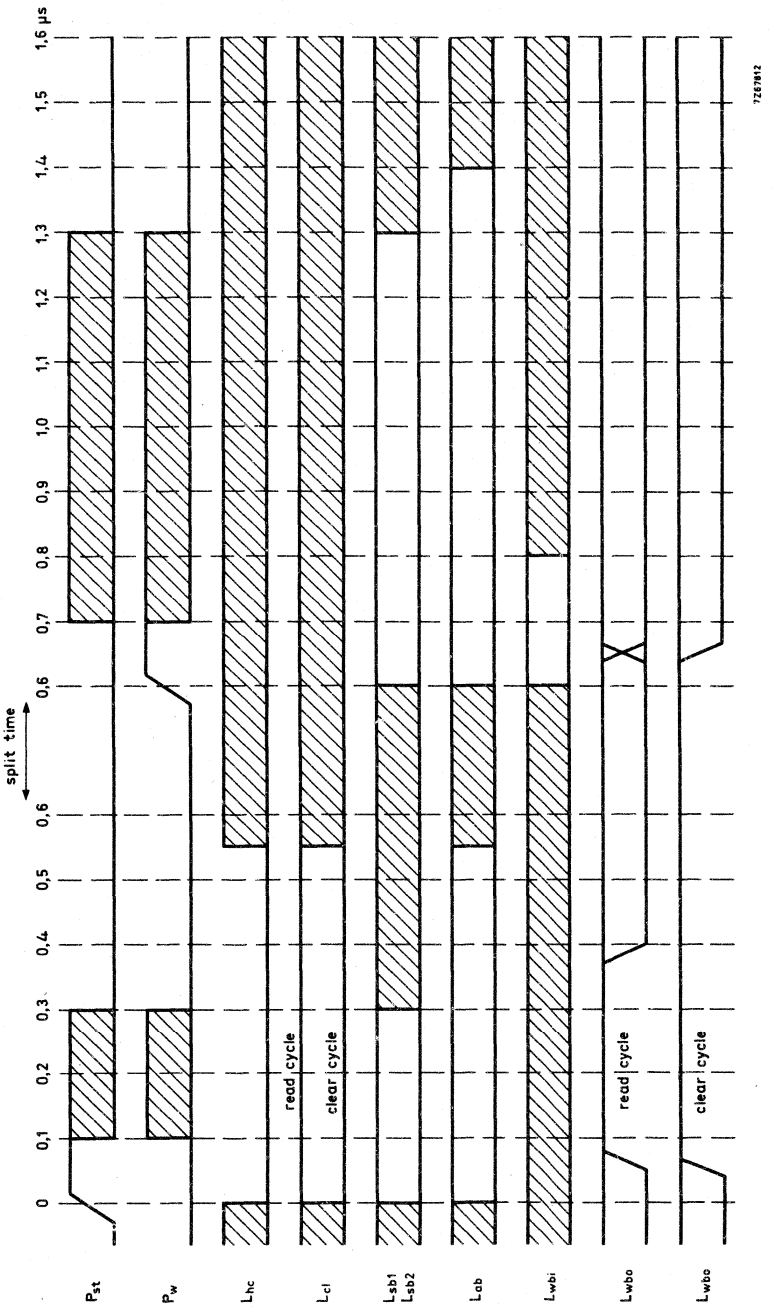
Timing diagrams



Interpretation of timing signals on the following pages.
Upper levls are "1", lower levels are "0".



Timing of read/restore and clear/write (full cycle) modes.



Timing of split cycle modes

1 μs CORE MEMORY SYSTEM

QUICK REFERENCE DATA	
Capacity	1 k/13 extendable to 16 k/13
Cycle time	1 μs
Access time	0,5 μs
Data and address registers	
Memory retention	
DTL/TTL compatible	
Random access	
Single power supply	+5 V

DESCRIPTION

A 3D, 3-wire complete random access core memory system, built on 3 printed-wiring boards. The system is fully TTL compatible both for the logic and the supply voltage, so it fits perfectly in all other TTL electronics. A memory retention circuit (including 5 V sensing) prevents data loss when power fails.

MECHANICAL DATA

Dimensions

width	26,8 mm
height	233,4 mm
depth	160 mm

Mounting

The components are mounted on three printed-wiring boards provided with plugs and sockets with which the electrical connections are made. The stack board is sandwiched between two electronics boards the components of which are mounted on the inside. On the long side the assembly is provided with two connector parts F068 with 64 pins for interfacing.
The memory will fit a standard Europe board rack.

ENVIRONMENTAL DATA

Ambient temperature range,	operating	0 to +65 °C
	non-operating	−40 to +85 °C
Humidity		up to 90% (without condensation)
Shock		18 shocks of 50 g each of 11 ms duration
Vibration		5 to 150 Hz at 2 g or a maximum amplitude of 2,5 mm peak-to-peak, duration 6 h.
Cooling		an air flow of 50 l/min is required.

ELECTRICAL DATA

Memory capacity

number of words	number of bits/word
1024	13

A maximum of 16 memory modules can be paralleled to give a capacity of 16 k/13.

Memory speed (see also timing diagrams)

mode of operation	cycle time	access time
read/restore	1 µs	0,5 µs
clear/write	1 µs	

Input signals

CI (and $\overline{CI}$)	cycle inititiate (bipolar to reduce noise sensitivity)
MC	mode control (determines read/restore and clear/write cycle)
AB_n	address information (n = 0...9)
AB_{10}, AB_{11}	module selection bits, to select one out of four parallel 1 k/13 modules
BS_n	block selection inputs, to select one 4 k/13 block from a group of four (n = 1...4)
DE	enable signal (enables inverted data out signals)
DI_n	data input (n = 1...13)

Output signals

DA	data available
DO_n	data output signals
$\overline{DO}_n$	inverted data output signals

Interface

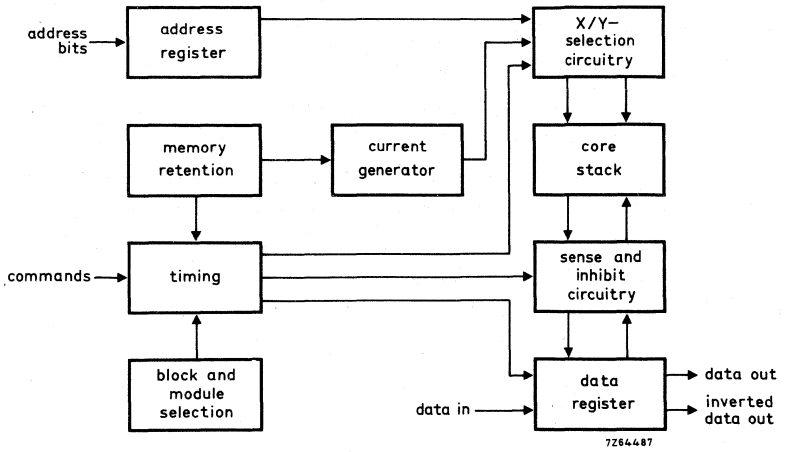
Input and output levels "1"	HIGH TTL level
"0"	LOW TTL level

Interface connections are made via two connectors F068.

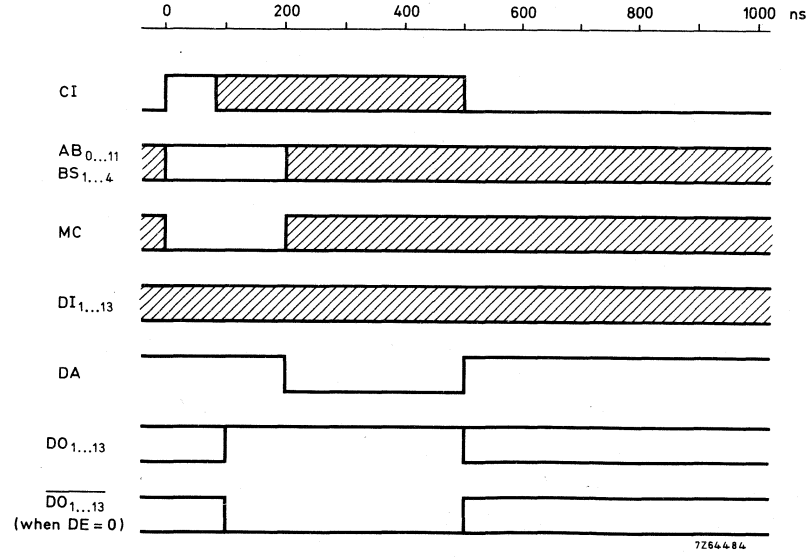
Power supply requirements

Supply voltage, operating tolerance	+5 V, ± 5%
Current consumption	
stand-by	max. 3,4 A
operating	max. 6 A
Safety margin	+10%

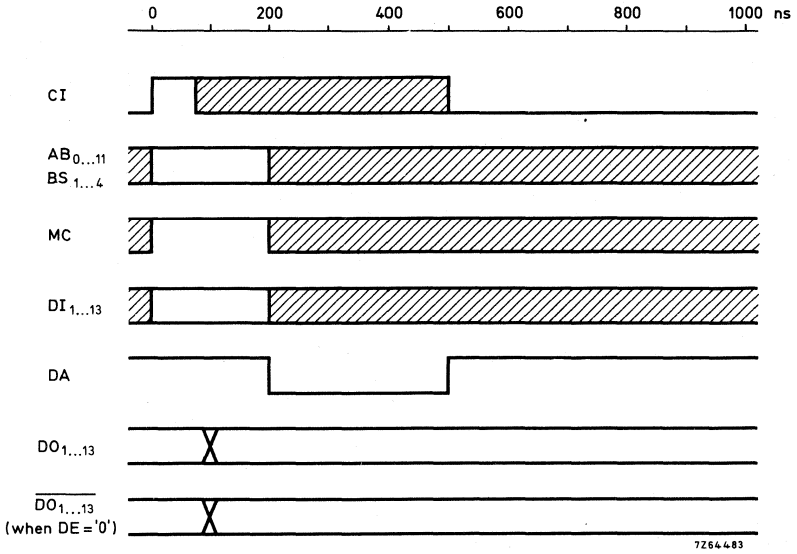
Memory contents



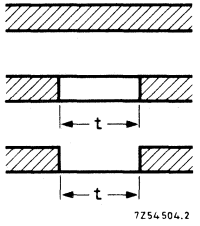
Timing diagrams



Timing of read/restore mode.
For interpretation of timing signals, see the figure on the next page.



Timing of clear/write mode.



don't care

input level must be defined
output level can be either
"1" or "0".

level as indicated

Interpretation of timing signals

IDENTIFICATION

Core memory system FI-26, catalogue number 2722 105 20400
Mating connector part F068, catalogue number 2422 025 89288 and 2422 025 89298

For ordering purposes please quote the 12-digit catalogue number.
The mating connector parts have to be ordered separately.

0,65 and 0,7 µs CORE MEMORY SYSTEMS

QUICK REFERENCE DATA		
	FI-68	FI-69
Basic capacity	8 k 18	16 k 18
Full cycle time	0,65 µs	0,7 µs
Access time	0,26 µs	0,3 µs
Interface	TTL/DTL	
Supply voltages	+5 and +15 V	
Dimensions	160 x 233 x 36 mm	160 x 233 x 42 mm

DESCRIPTION

The FI-68 and FI-69 are high-speed mini memories having basic capacities of 8 k 18 and 16 k 18 respectively, which can be expanded to eight times as much by adding further memory modules. The use of separate memory and control modules means economy and flexibility.
The 3D3-wire system, built around a continuously wired core stack, the advanced design featuring the lowest possible dissipation, makes these memories very compact and reliable.

MECHANICAL DATA

All components, including the core stack, are mounted on glass epoxy printed-wiring boards. The boards are electrically interconnected by plugs.
The control module and one board of the memory module are equipped with two F068 connectors in accordance with the Euro-standards for external interface.

Dimensions

	FI-68	FI-69
Width	36 mm	42 mm
Height	233 mm	233 mm
Depth	160 mm	160 mm
Number of printed-wiring boards	3	4

ENVIRONMENTAL DATA

Ambient temperature range	0 to +55 °C
Humidity	up to 90% (without condensation)
Shock	10 g
Vibration	5 to 55 Hz at 2 g or a maximum amplitude of 3 mm peak-to-peak
Cooling	by forced air, 10 l/s

ELECTRICAL DATA

	FI-68	FI-69
Basic capacity	8 k 18	16 k 18

Memory speed

mode of operation		FI-68 cycle time	FI-68 access time	FI-69 cycle time	FI-69 access time
read/restore	full cycle	0,65	0,26	0,7	0,3
clear/write	full cycle	0,65		0,7	
read/modify/write,	split cycle	0,8	0,26	0,85	0,3

Interface

Input signals:

RI	read initiate
$\overline{WI}$	write initiate
$\overline{FC}$	full/split cycle
AI_{00-17}	address information
$\overline{DI}_{00-17}$	data input
$\overline{BC}_{1-2}$	byte control
DOS_{1-2}	data output strobe
DS	data save
MEM SEL	memory selection
MR	master reset
FHW	full/half word

Output signals:

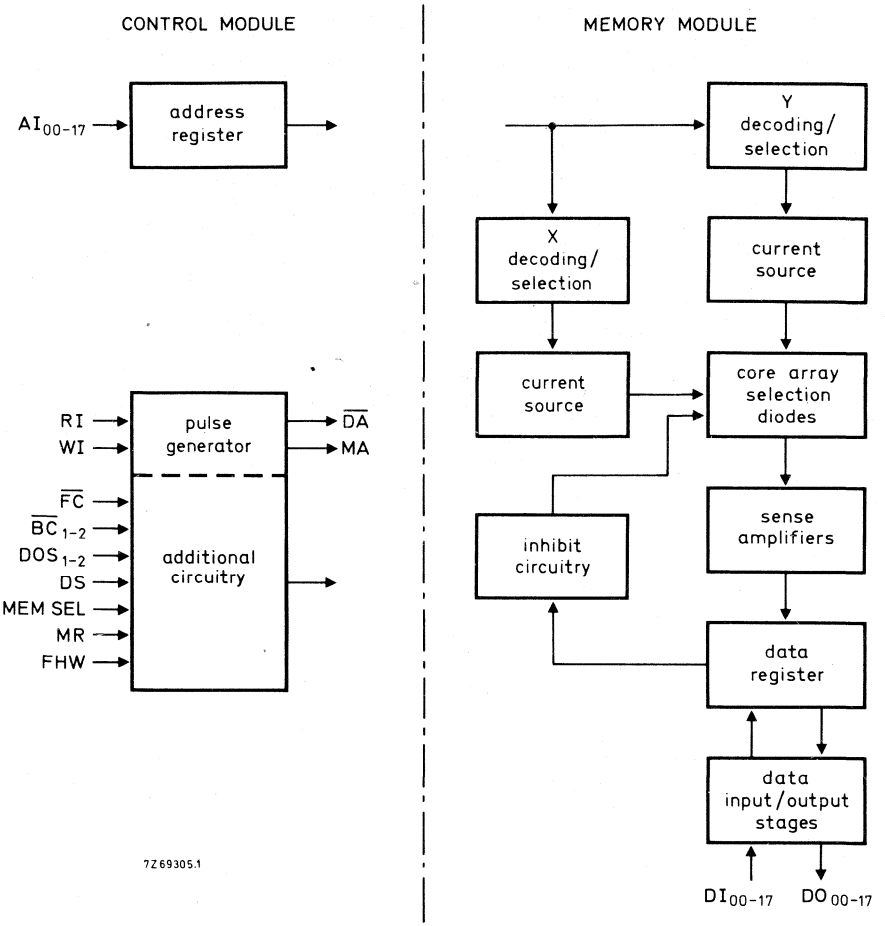
$\overline{DO}_{00-17}$	data output
DA	data available
MA	memory available

Signal levels : TTL compatible

Power supply requirements

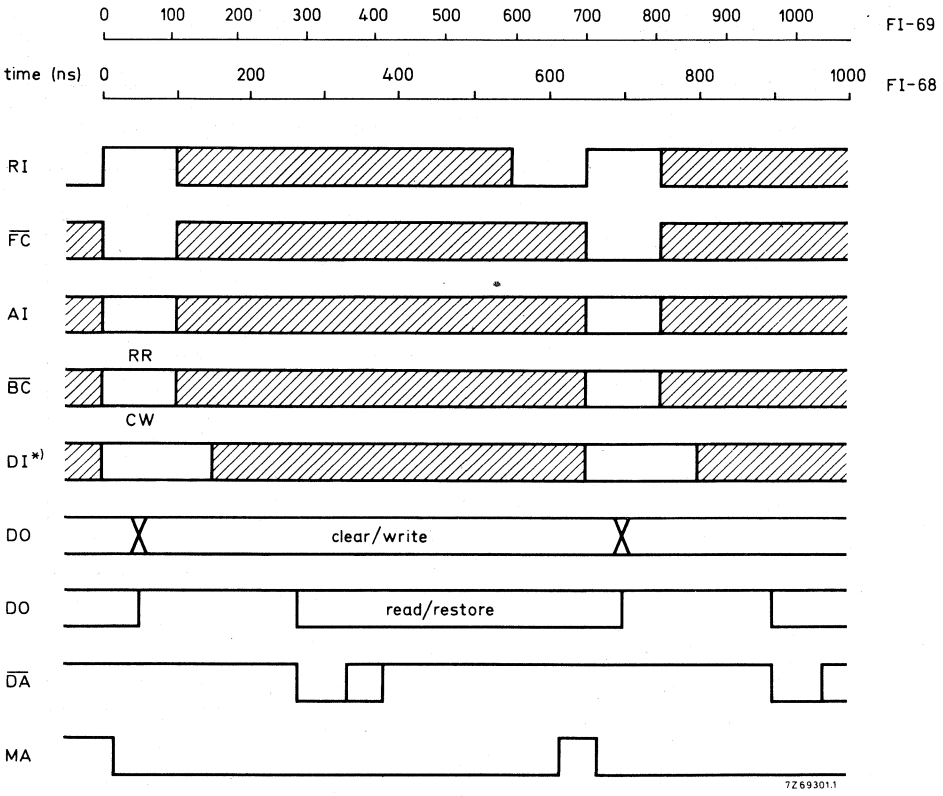
		+5 V FI-68	+5 V FI-69	+15 V FI-68	+15 V FI-69
control module	standby current	1,0 A	1,2 A	0,07 A	0,07 A
	operating current	1,0 A	1,2 A	0,1 A	0,1 A
memory module	standby current	1,2 A	1,5 A	0,1 A	0,1 A
	standby current, selected	2,1 A	2,2 A	0,1 A	0,1 A
	operating current	2,4 A	2,5 A	4,0 A	4,7 A

Memory contents

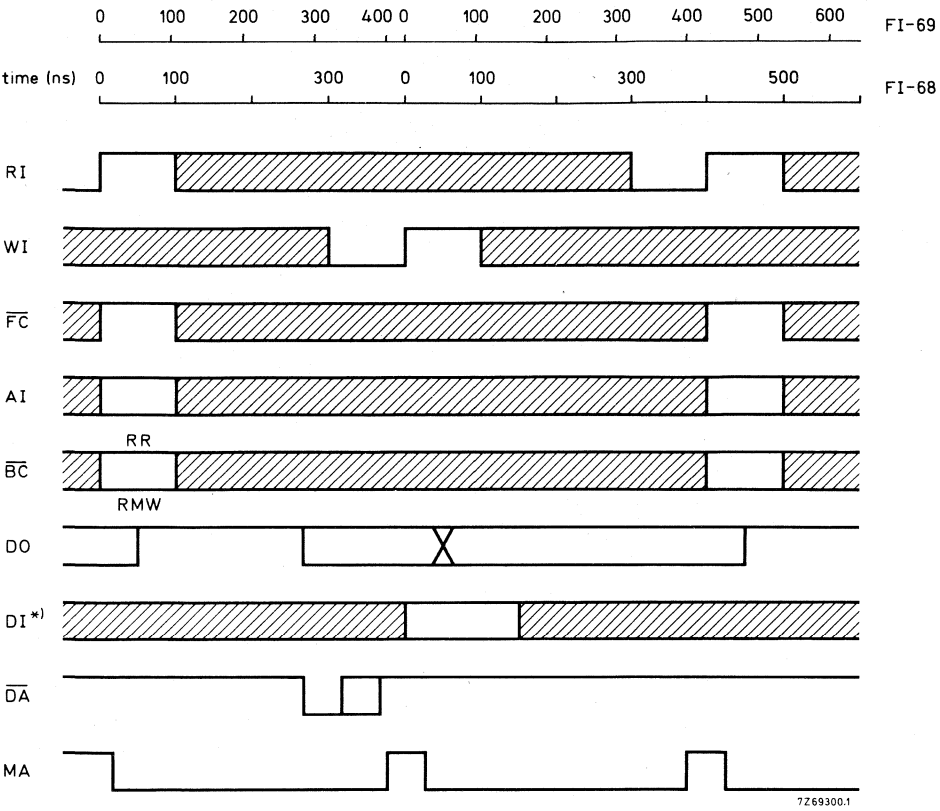


Block diagram

Timing diagrams



Full cycle (read/restore, clear/write).
*) Specified for clear/write; DI is don't care in read/restore.



Split cycle (read/restore, read/modify/write).
*) Specified for read/modify/write; DI is don't care in read/restore.

IDENTIFICATION

type	catalogue number	
	control module	memory module
FI-68	4322 027 69970	4322 027 69550
FI-69	4322 027 68970	4322 027 68980

Catalogue number of mating connector: 2422 025 89288 (pins for wire wrap)
2422 025 89298 (solder pins)

For ordering purposes please quote the catalogue number.

0,75 µs CORE MEMORY SYSTEM

QUICK REFERENCE DATA	
Capacity	from 4 k/18 to 32 k/18 16- and 12-bit modules available by means of component stripping
Cycle time	0, 75 µs
Access time	0, 3 µs
Address register	
Data input/output register	
TTL/DTL compatible	
Byte control on 9, 8 or 6 bits (for 18, 16 or 12 bit system respectively)	
Data save input	

DESCRIPTION

The FI-75 is a random access core memory system with 18 mil cores in a 3D three-wire configuration. The system has a basic capacity of 4k words of 18 (16, 12) bits, and consists of a memory control board and a memory module.

The control board carries the timing circuitry, address register, data input/output register and inhibit resistors, while it is capable of driving up to eight memory modules. Thus the maximum available capacity is 32k words of 18(16, 12) bits each.

MECHANICAL DATA

The memory module is built on two printed-wiring boards which are linked mechanically by means of flexible combs and are folded together. The memory control board and the memory module are connected externally via two pairs of F061 – F062 connector combinations. The boards can be mounted horizontally or vertically in a chassis. The system can be made suitable for plug-in connection by means of board guides.

Dimensions

	memory module	memory control
Width	34 mm	17 mm
Height	208 mm	208 mm
Depth	310 mm	310 mm

ENVIRONMENTAL DATA

Ambient temperature range	0 to 50 °C
Humidity	up to 90 % (without condensation)
Shock (memory plugged in)	1000 bumps of 2 g
Vibration	5 to 150 Hz at 1 g max.
Cooling	an air flow of 600 l/min is required to cool the memory system

ELECTRICAL DATA

Memory capacity

number of words	number of bits/word
4096	18
4096	16
4096	12

Memory speed (see also timing diagrams)

mode of operation		cycle time	access time
read/restore	full cycle [1]	0,75 µs	0,3 µs
clear/write	full cycle [1]	0,75 µs	
read/modify/write	split cycle [1]	0,77 µs	0,3 µs
clear/write	split cycle [1]	0,75 µs	
read/restore	split cycle [1]	0,75 µs	0,3 µs

Input signals

RR	read-request, start command for full cycle and read/clear operation in split cycle
WR	write request, start command for write operation in split cycle
BS	block selection, to select one block of 32 k from several blocks
AB_n	address information (n = 0...14)
DI_n	data input (n = 0...17)
DS	data save; prevents loss of information during switch-on/switch-off
CB_0 and CB_1	byte control during read/clear in full-and split cycle operation
NW_0 and NW_1	byte control during write in split cycle operation

Output signals

DO_n	data output (n = 0...17)

[1]) It depends on the back wiring whether full or split cycles are made.

Interface

TTL/DTL compatible

Interconnections	via twisted pairs
Input and output levels	"1" HIGH TTL level "0" LOW TTL level

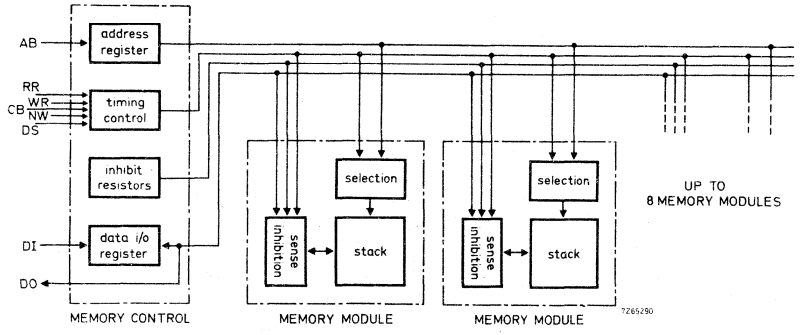
All input signals have terminating resistors.

Power supply requirements

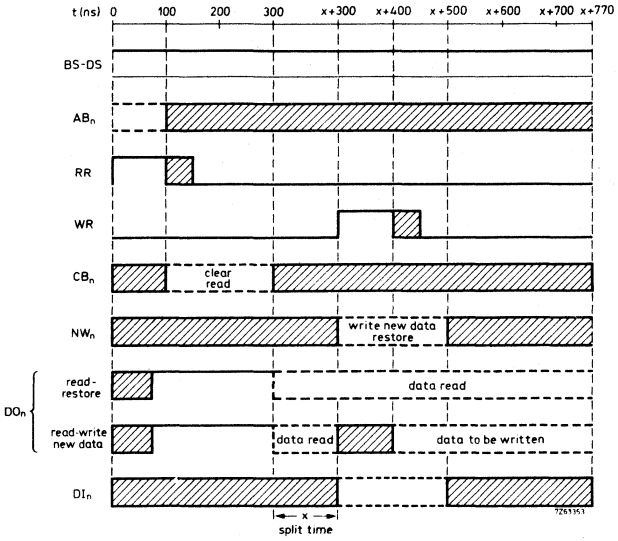
voltage (V)	max. stand-by current (A)		max. current (A)		operating tolerance (%)	safety margin (%)	max. dI/dt (A/µs)
	16 bits	18 bits	16 bits	18 bits			
+24	0,8 n	0,9 n	4,5 + 0,8 n	5,0 + 0,9 n	± 2	± 7	0,5
+ 5	1,5 + 1,0 n	1,6 + 1,1 n	1,5 + 1,0 n	1,6 + 1,1 n	± 5	± 10	0,002
- 5	0,20 n	0,20 n	0,20 n	0,20 n	± 5	± 15	0

Note - n is the number of memory modules driven by one memory control board.

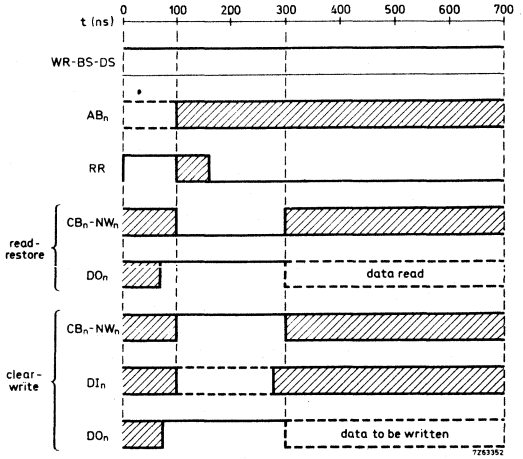
Memory contents



Timing diagrams



Timing diagram split cycle



Timing diagram full cycle

IDENTIFICATION

type	catalogue number
4k18 memory module	4311 027 72800
4k18 memory control	4311 027 08670
4k16 memory module	4311 027 72860
4k16 memory control	4311 027 08700
4k12 memory module	4311 027 72820
4k12 memory control	4311 027 08720
mating connector F061	2422 061 63131

For ordering purposes please quote the 12-digit catalogue number.
The mating connectors have to be ordered separately.

1,5 μs CORE MEMORY SYSTEMS

QUICK REFERENCE DATA	
Capacity, FI-128	4 k/8
FI-138	8 k/8
FI-148	16 k/8
Cycle time	1,5 μs
Access time	0,6 μs
TTL compatible	
Data and address registers	
Data save circuitry	
Module selection	
Random access	

DESCRIPTION

A family of ferrite core memories for random access, consisting of the FI-128, FI-138 and FI-148, having a capacity of 4k, 8k and 16k words of 8 bits, respectively.

The application of low-drive 18 mil cores in an economic 3D three-wire organization, and the use of TTL integrated circuits and silicon semiconductors form a guaranty for maximum compactness and reliability of the memory units.

MECHANICAL DATA

Dimensions

	FI-128	FI-138	FI-148
Width	45 mm	55 mm	55 mm
Height	233,4 mm	233,4 mm	233,4 mm
Depth	220 mm	220 mm	220 mm

Construction

All components are mounted on three glass epoxy printed-wiring boards of the standard Europe type, plugged together to form a self-contained unit which can slide into a mounting chassis. One of the boards has been provided with a connector part F068 with 2 x 32 pins for interface connections.

ENVIRONMENTAL DATA

Ambient temperature range	0 to +55 °C
Humidity	up to 90% (without condensation)
Shock	10 g during 11 ms
Vibration	5 to 55 Hz at 1 g or a maximum amplitude of 2,5 mm peak-to-peak
Cooling	by forced air, 300 l/min.

ELECTRICAL DATA

Memory capacity

type	number of words	number of bits/word
FI-128	4096	8
FI-138	8192	8
FI-148	16384	8

Memory speed (see also timing diagrams)

mode of operation	cycle time	access time
read/restore	1,5 µs	0,6 µs
clear/write	1,5 µs	

Interface signals

PS	start command
PL	address accept signal
PA	address information
PE	memory enable input
PC	mode of operation level
PD	data input/output
PR	data save input
PQ	data available/end of cycle

Interface levels

PR LOW ≤ 0,8 V
HIGH ≥ 3,75 V

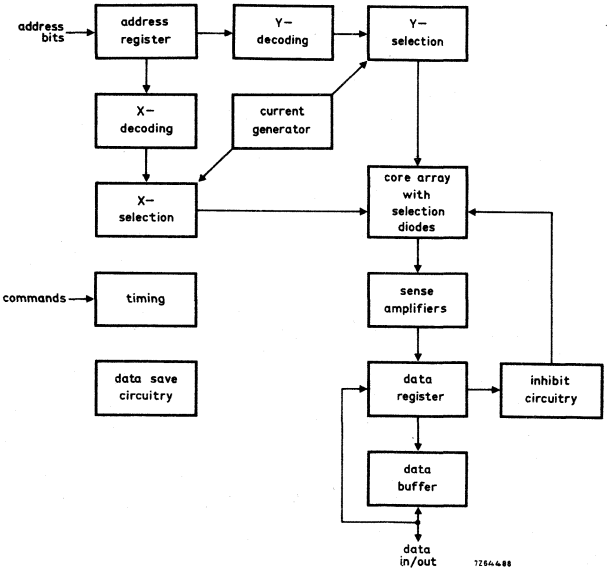
All other signals are TTL/DTL compatible.

Power supply requirements

supply voltage	max. stand-by current			max. operating current		
	FI-128	FI-138	FI-148	FI-128	FI-138	FI-148
+ 5 V	1,5 A	1,5 A	1,5 A	1,5 A	1,5 A	1,5 A
- 12 V	0,2 A	0,2 A	0,2 A	0,2 A	0,2 A	0,2 A
+ 12 V	0,5 A	-	-	3,5 A	-	-
+ 16 V	-	0,5 A	0,5 A	-	3,5 A	3,5 A

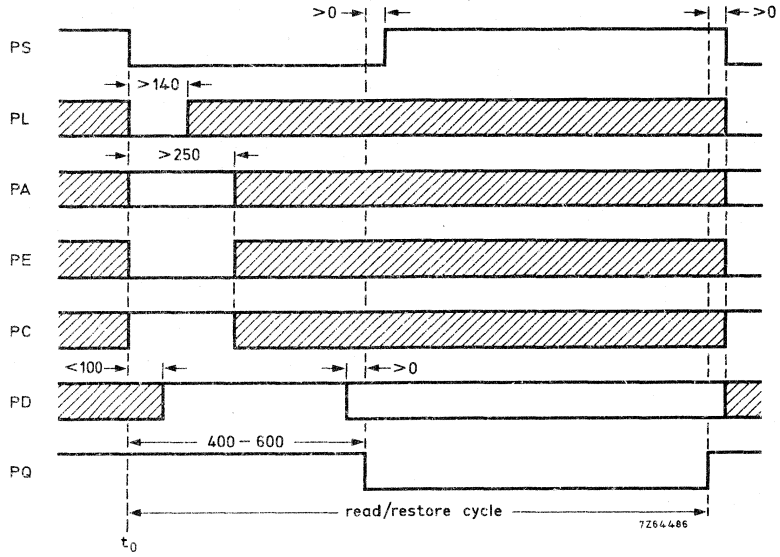
Notes - The current values are maximum ones under worst case conditions.
- The operating tolerances of the power supplies are ± 5%.
- The safety margins are + 10%.

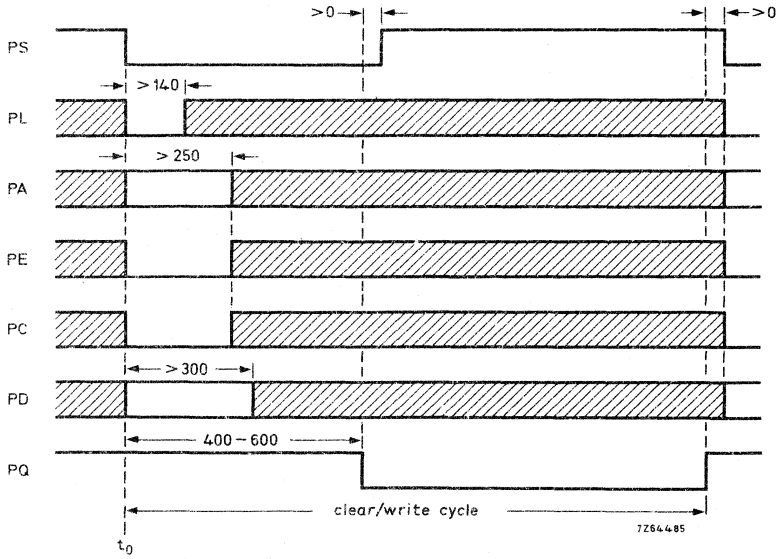
Memory contents

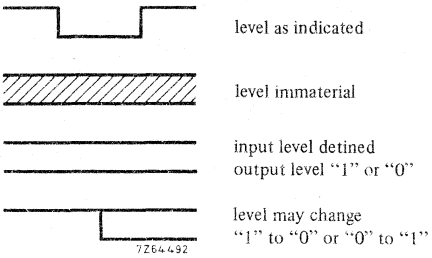


Block diagram

Timing diagrams







Interpretation of timing signals

IDENTIFICATION

type	catalogue number of	
	core memory	instruction manual
FI-128 (4 k/8)	2722 103 10011	4322 027 65890
FI-138 (8 k/8)	2722 103 10211	4322 027 65900
FI-148 (16 k/8)	2722 103 10411	4322 027 65900

Mating connector part F068, with 2 x 32 pins, catalogue number 2422 025 89286

For ordering purposes please quote the 12-digit catalogue number.
The mating connector part and the instruction manual have to be ordered separately.

1,2 μs CORE MEMORY SYSTEMS

QUICK REFERENCE DATA		
	FI-1316	FI-1416
Basic capacity	8 k 16	16 k 16
Cycle time	1,2 μs	1,2 μs
Access time	0,45 μs	0,46 μs
Interface	TTL/DTL	
Supply voltages	+5 V, −5 V, +16 V	
Dimensions	421 x 362 x 13 mm	

DESCRIPTION

The FI-1316 and FI-1416 are single board memories intended for mainly mini computers. The address circuitry provides capacity expansion up to eight times the basic capacity. Facilities for bus interface are provided. The memory operates asynchronously. Mounting the 3D-3 wire continuously wound core stack direct on the memory board results in an extremely flat construction with an overall thickness of no more than 0,5 in.

MECHANICAL DATA

Dimensions in mm

Width	421 mm
Height	13 mm
Depth	362 mm

The long side of the memory is fitted with an edge connector with 2 x 43 contacts (0,1 in pitch) for external interface.

ENVIRONMENTAL DATA

Ambient temperature range	0 to +50 °C
Humidity	up to 90% (without condensation)
Shock	15 g
Vibration	5 to 150 Hz at 1 g or a maximum amplitude of 0,25 mm peak-to-peak
Cooling	by forced air

ELECTRICAL DATA

		FI-1316		FI-1416	
Basic capacity		8 k 16		16 k 16	
Memory speed					
mode of operation		cycle time	access time	cycle time	access time
read/restore	full cycle	1,2 μs	0,45 μs	1,2 μs	0,46 μs
clear/write	full cycle	1,2 μs		1,2 μs	

Interface signals

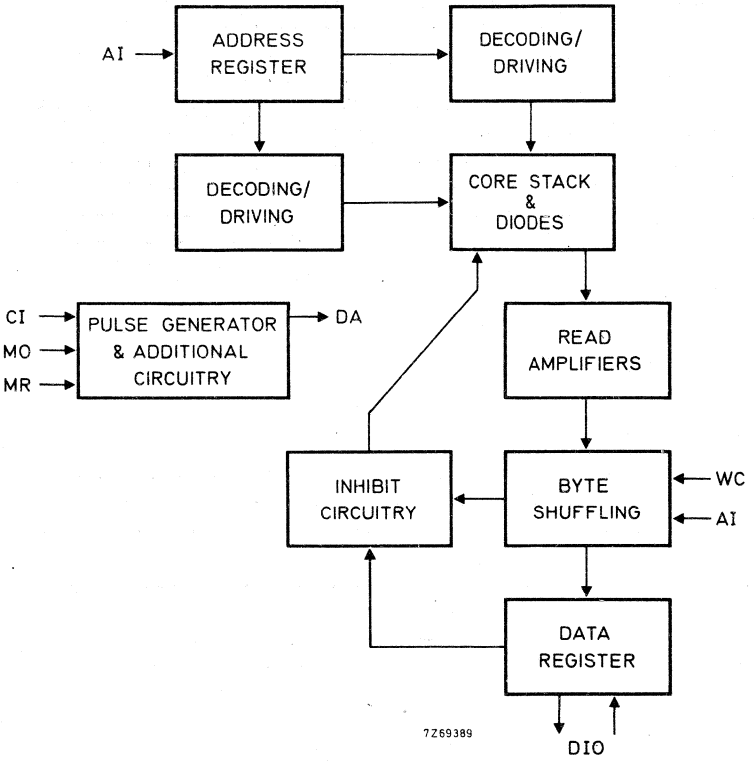
CI	cycle initiate
MO	read/restore, clear/write
WC	word/character exchange
AI	address information
DIO	data input/output
MR	memory release
DA	data available

Interface levels: TTL compatible

Power supply requirements

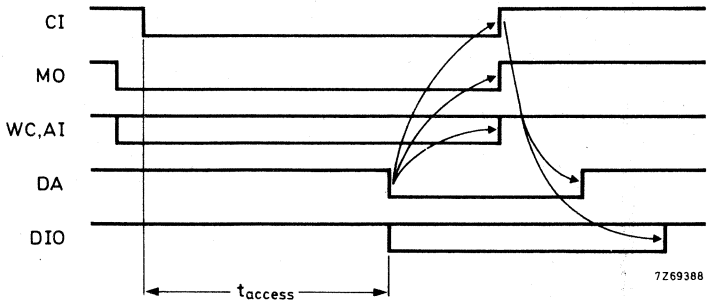
supply voltage	FI-1316		FI-1416	
	standby current	operating current	standby current	operating current
+5 V	3,1 A	3,4 A	3,7 A	4,2 A
−5 V	0,2 A	0,2 A	0,4 A	0,4 A
+16 V	0,6 A	4,5 A	0,7 A	4,6 A

Memory contents

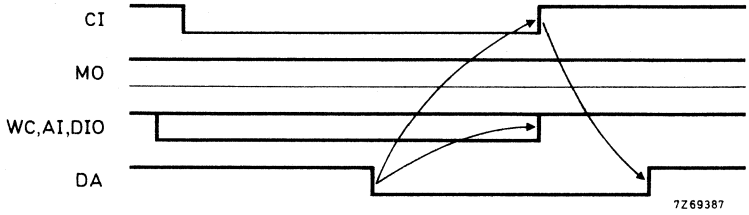


Block diagram

Timing diagrams



Timing of read/restore mode



Timing of clear/write mode

IDENTIFICATION

type	catalogue number
FI-1316	4311 027 73060
FI-1416	4322 027 69690

For ordering purposes please quote the catalogue number.

0,75 µs CORE MEMORY SYSTEMS

QUICK REFERENCE DATA	
Capacity	4k-16k/12-36
Expandability	4 memory systems in parallel
Cycle time	0,75 µs
Access time	0,3 µs
TTL/DTL compatible	
Memory retention	
Mains supply voltage (a.c.)	110 V, 220 V
Mounting	in standard 19 in rack

DESCRIPTION

The PRM-7 family is a range of stand alone memory systems, based on the 0,75 µs core memory system FI-75.
The memory systems are housed in cabinets, which are suitable for mounting in a 19 in rack. A cabinet can house up to four memory modules, one control module and one optional interface board, on which the customer can mount its own electronics. It contains also the two power supplies including memory retention circuitry, the blowers and the interface connectors mounted at the back panel. Due to the advanced power supply design the proper functioning of the memory system is not affected by mains interruptions as long as 20 ms at maximum load and the mains voltage at its lower limit. Two switches mounted inside the cabinet allow the check of the memory functions at marginal power supply voltages.

MECHANICAL DATA

Dimensions

Width	442 mm	(17,5 in)
Height	133 mm	(5,25 in)
Depth	425 mm	(16,75 in)

Construction

The memory modules, control module and interface board can be plugged horizontally into the cabinet from the front side. The back panel can be hinged along its horizontal axis to give access to the interface wiring and the marginal check switches. The 3-pins mains plug and fuse are located at the left side of the back panel. The memory system has three 50-pins interface connectors; optionally six more connectors can be mounted to satisfy special interface requirements of the customer. Two blowers are located at the right side of the cabinet.

ENVIRONMENTAL DATA

Ambient temperature range	0 to + 50 °C
Humidity	up to 90% without condensation
Cooling	by built in blowers

ELECTRICAL DATA

Memory capacity

number of words	number of bits/word
4096	12, 16, 18, 24, 32 or 36
8192	12, 16, 18, 24, 32 or 36
16384	12, 16, 18

Expandability: 4 memory systems in parallel

Memory speed

mode of operation		cycle time [1]	access time
read/restore	full cycle (standard)	0,75 µs	0,3 µs
clear/write	full cycle (standard)	0,75 µs	
read/modify/write	split cycle (optional)	0,75 µs	0,3 µs
read/restore	split cycle (optional)	0,75 µs	0,3 µs
clear/write	split cycle (optional)	0,75 µs	

Input signals

RR	read request
WR	write request
BS	block selection
AB_n	address information
DI_n	data input
CB_0 and CB_1	clear byte — these signals control the
NW_0 and NW_1	new write — operation per byte

Output signals

DO_n	data output

Interface

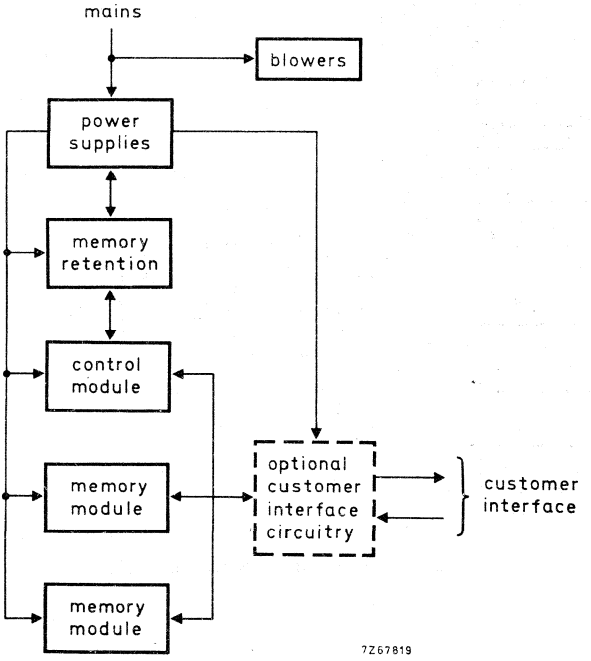
TTL/DTL compatible
A customer interface circuitry can be mounted on the optional interface board. This board is normally supplied without components.

[1]) For 24, 32 and 36 bits versions the cycle time is 0,8, 1,05 and 1,15 µs respectively.

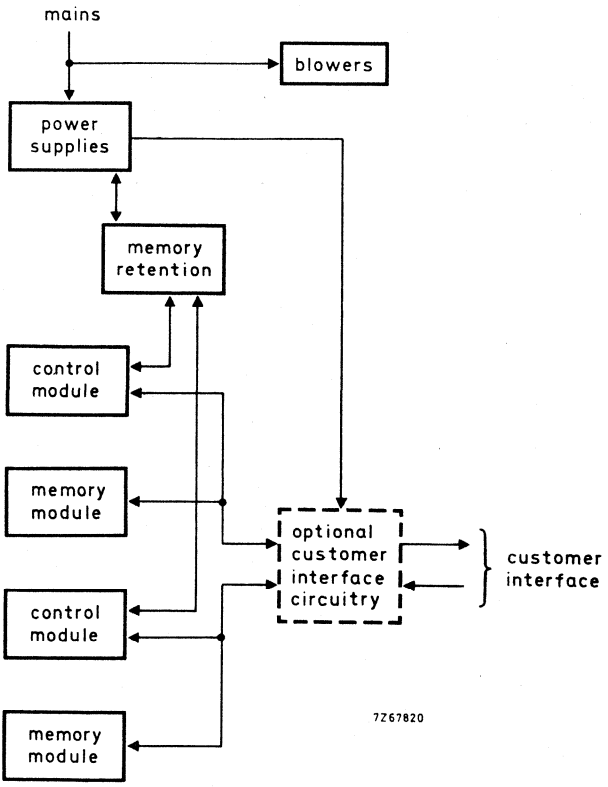
Power supply requirements

Input voltage	110 V/220 V, +15%, −30%, 250 W, 47 to 63 Hz ; optional : 400 Hz 48 V d.c.
Output voltage	+24 V, 8 A ± 2% + 5 V, 15 A ±2% − 5 V, 1 A ± 5%

Memory contents

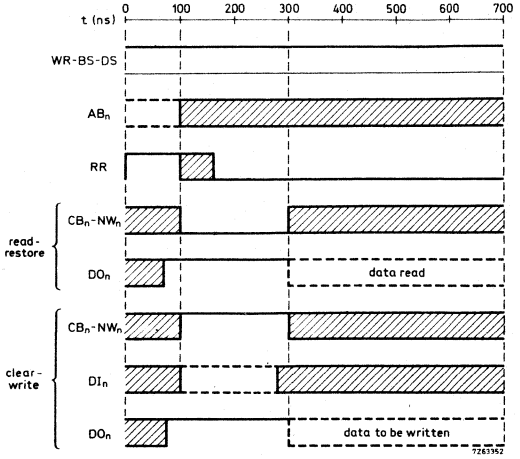


Block diagram, 8k/18 configuration

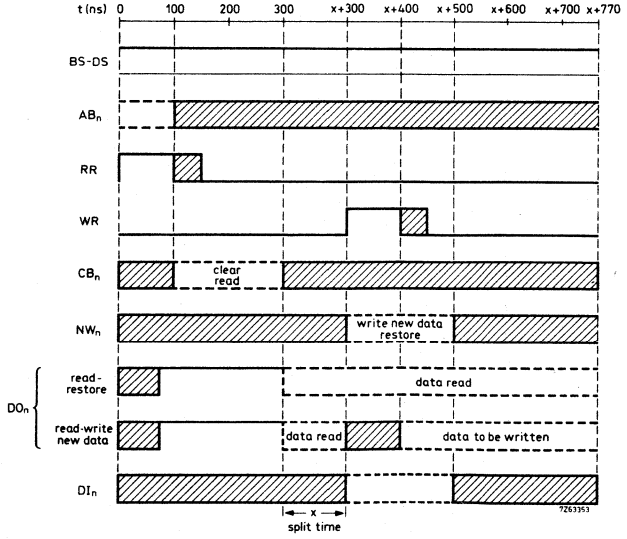


Block diagram, 4 k/36 configuration

Timing diagrams



Timing diagram full cycle



Timing diagram split cycle

1,4 µs CORE MEMORY SYSTEMS

QUICK REFERENCE DATA	
Basic capacity	16 k/36
Modularity [1]	16 k/36
Maximum capacity	128 k/36 or 16 k/288
Cycle time	1,4 µs
Access time	0,6 µs
TTL/DTL compatible	
Data and address registers	
Byte control	
Memory retention	

DESCRIPTION

A ferrite core memory system for random access with capacities ranging from 16 k/36-bit words to eight times as much (4,8 million bits) in any configuration. By making use of the byte control inputs the basic module (16 k/36) can also be operated as 32 k/18 or 64 k/9; moreover provisions are included for interleaved mode of operation of several memories. The capacity of any configuration of Q14 memory modules (except the largest) can be expanded by simply adding another memory module which shares the same control module. Using TTL integrated circuits and silicon semiconductors in conjunction with a continuously wired core array, the memory is highly compact and of supreme reliability.

MECHANICAL DATA

Dimensions

	memory module	control module
Width	50 mm	20 mm
Height	292 mm	292 mm
Depth	365 mm	365 mm

Mounting

All components mounted on epoxy glass printed circuit boards. The memory module consists of four printed circuit boards (two electronics boards plug-connected to two folded stack boards). The control module consists of only one printed circuit board.

1) Increments of capacity expansion.

ENVIRONMENTAL DATA

Ambient temperature	0 to 55 °C
Humidity	up to 90 % (without condensation)
Shock	10 g in all main directions
Vibration	5 to 150 Hz at 1 g or an amplitude of 3 mm peak-to-peak
Cooling	by forced air (1300 l/min)

ELECTRICAL DATA

Memory capacity

	number of words	number of bits/word
basically	16 384	36
expandable to modularity	16 384	288
	131 072	36
	16 384	36

Memory speed (see also timing diagrams)

mode of operation	cycle time	access time
clear/write	1,4 µs	
read/restore	1,4 µs	0,6 µs
read/modify/write(split time)	1,4 µs	0,6 µs

Input signals

$\overline{RR}$ read request
$\overline{WR}$ write request
FSC cycle control
AB address information
DI data input
BC byte control
BI byte interleave
BS block selection
MS module selection

Output signals

DO data output
$\overline{DA}$ data available
MR memory ready
$\overline{MB}$ memory busy
LBC level byte control

Interface

TTL/DTL compatible

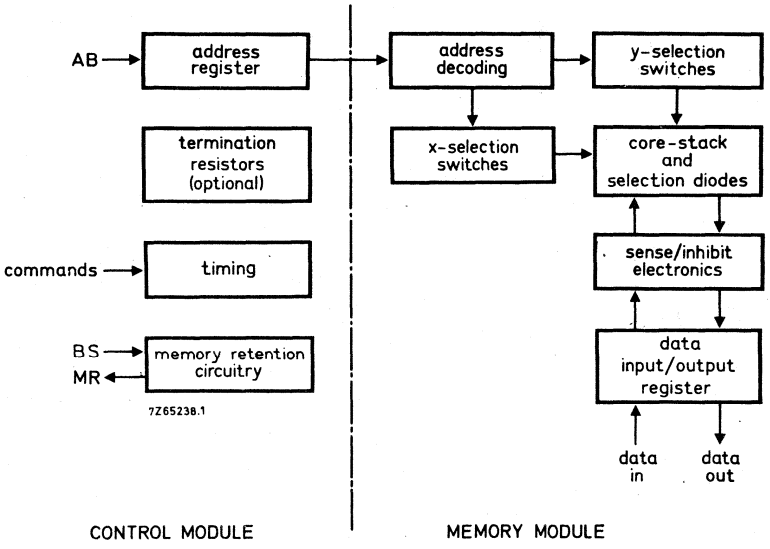
Interconnections		via 64-pin connectors F081 (4 connectors of the memory module 2 connectors of the control module)
Input levels	"1"	2,2 to 5,5 V
	"0"	0 to 0,4 V
Output levels	"1"	max. 5,5 V (open collector)
	"0"	0 to 0,6 V

Power supply requirements (d.c.)

	voltage (V)	operational current (A)	stand-by current (A)
memory module (16k/36)	+ 20	0,55	0,10
	− 20	9,5	0,50
	+ 5	3,0	1,9
control module	+ 20	n. 0,15 + 0,5	0,5
	− 20	0,15	0,15
	+ 5	1,2	1,2

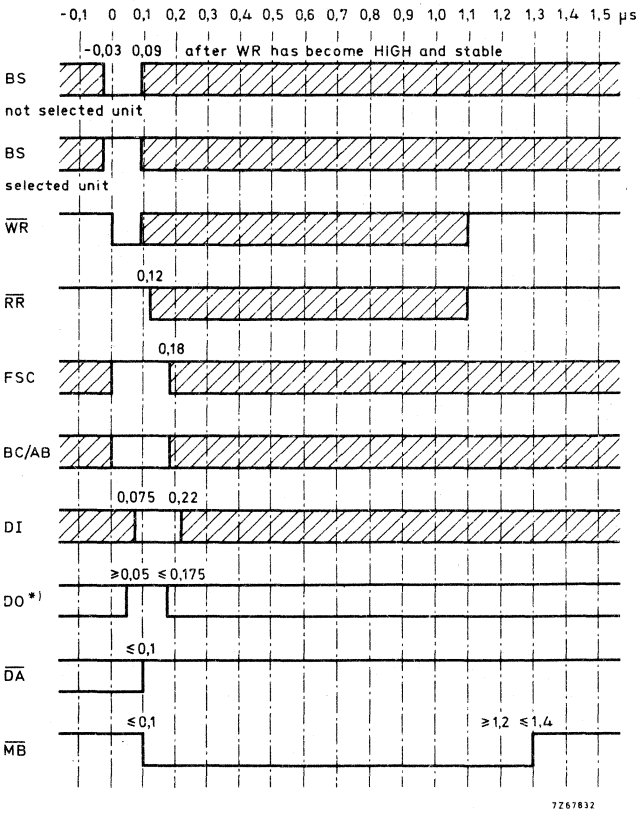
Notes– The currents are maximum values under worst case conditions.
n = number of memory modules driven simultaneously by one control module.

Memory contents



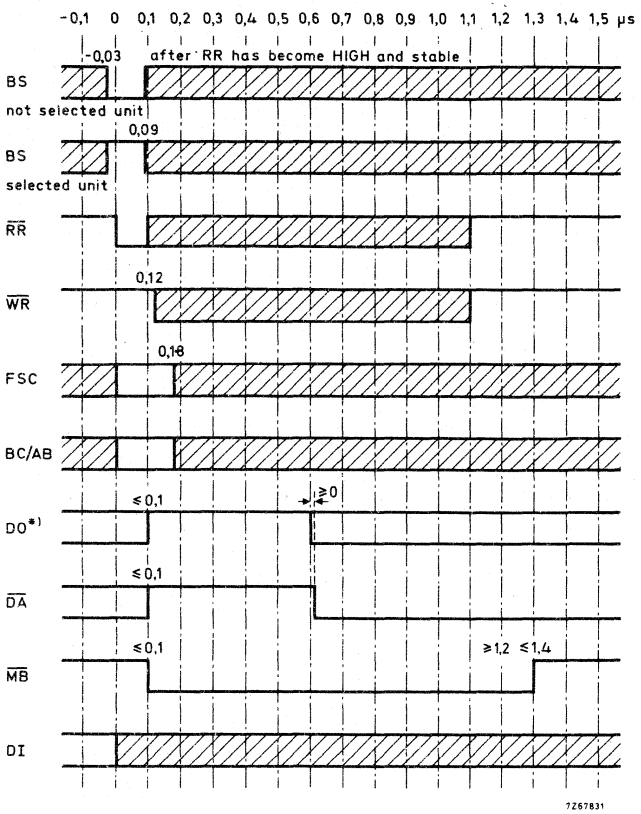
Block diagram

Timing diagrams

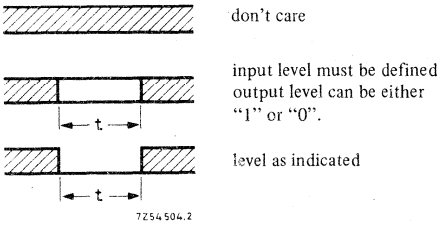


Clear/write cycle. For interpretation of timing signals, see the figure at the bottom of the next page.

*) The byte interleave (BI) input level decides whether the contents of the data register will be transferred to the data output stage or whether the data output stage will be kept in the HIGH position.



Read/restore cycle. See also the figure at the bottom of the page.



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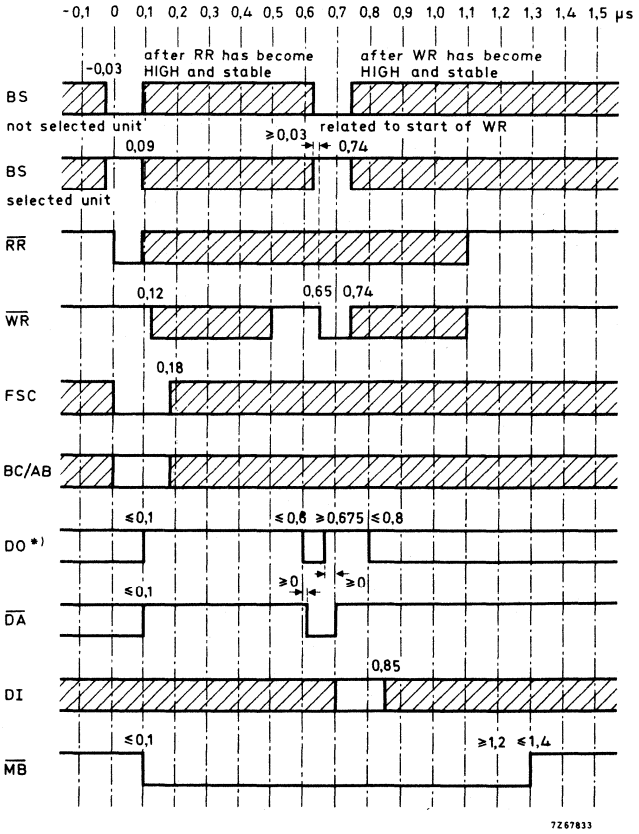

Read/modify/write cycle. After DA has become LOW a waiting (split) time can be introduced before starting the write phase. In that case all times after 0,65 µs and/or related to the start of the write phase have to be increased with this split time. Time indications as indicated above are based on a split time zero.

*) The byte interleave (BI) input level decides whether the contents of the data register will be transferred to the data output stage or whether the data output stage will be kept in the HIGH position.

IDENTIFICATION

type	catalogue number
control module (capable of handling up to eight memory modules)	4322 027 76310
memory module (capacity 16k/36)	4322 027 76320
manual	4322 026 57380

The catalogue number of the mating connector F081 is 2422 049 32001.

For ordering purposes please quote the 12-digit catalogue number. The mating connectors have to be ordered separately.

MAINTENANCE TYPE LIST

The types listed below are not included in this handbook.

Detailed information will be supplied on request.

FERROXCUBE MEMORY CORES

20H83 (6H3) 20H85 (6H5) 50C51 (6C1) 50C82 (6C2) 50D35 (6D5) 50D49 (6D9) 150E31 (6E1)	abridged date see table page A2

CORE MEMORY SYSTEMS

FI-2 FI-11 FI-12 FI-14	abridged data see table page C4

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